Progress Report of TOF Electronics

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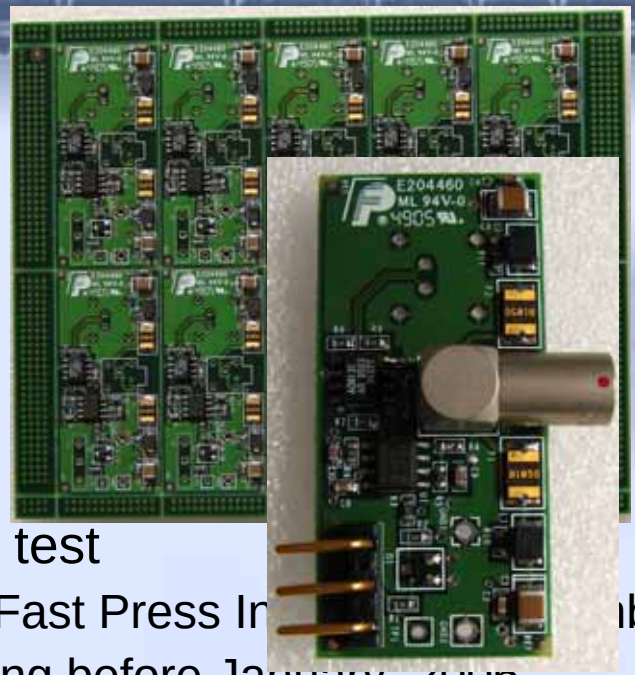
April 26, 2006

Outline

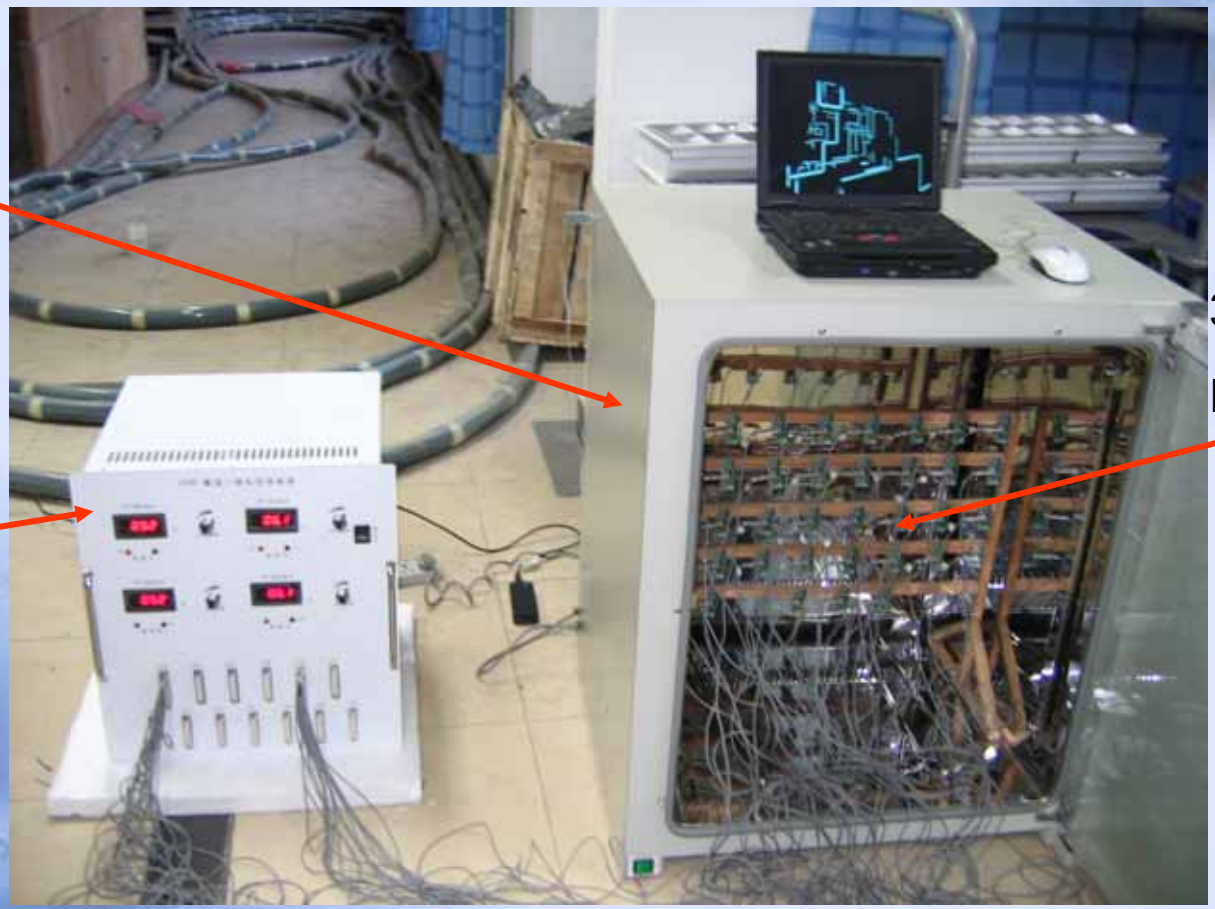
- The Status of TOF Readout Electronics
  - Mass production & heating aging for Pre-Amplifier
  - Design & test for Front End Readout Module Version 3
  - Modification for FEE_Rear Module
  - Upgrading for Clock Generator and Fanout Module
  - Modification for Fast_Control Module
  - ……
- The Status of TOF Trigger Electronics
  - Test for TOF Trigger Module
  - Design & test for Trigger_Rear Module

Pre-Amplifier



- Barrel Pre-Amplifier
  - 430 pieces are ready for test
    - PCB manufactured by Fast Press In ber, 2005
    - Mass soldered by Datang before January, 2006
  - Heating aging is in progress
    - Power Supply delayed for about 3 months
    - Process started on April 14, 2006
    - Scheduled to be finished before the end of July
- Endcap Pre-Amplifier
  - Being tested by Pro. Li Cheng now
  - Mass production is scheduled to begin before July

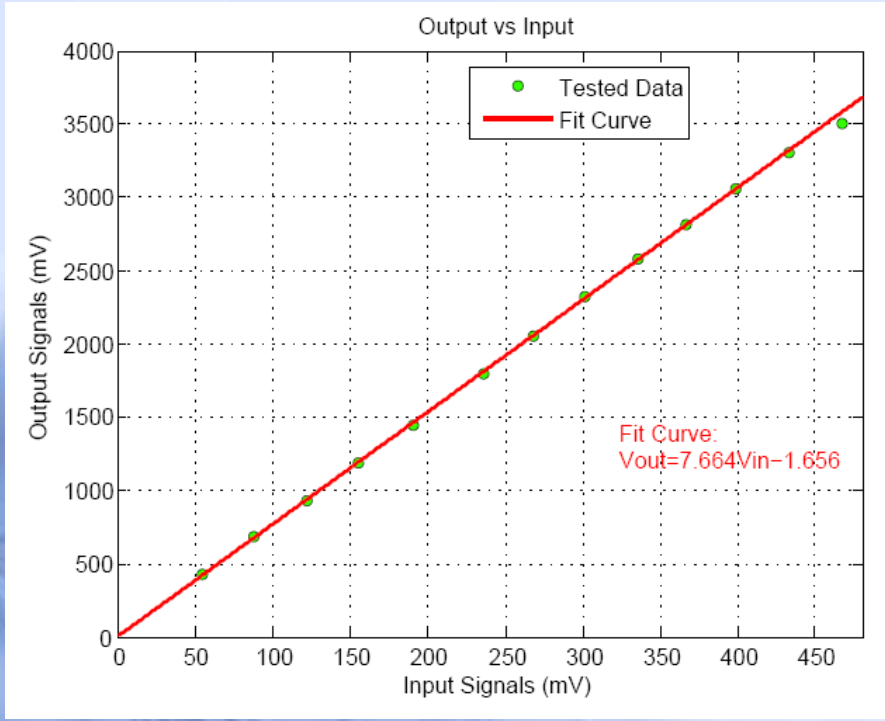
Heating Aging for Barrel Pre-Amp

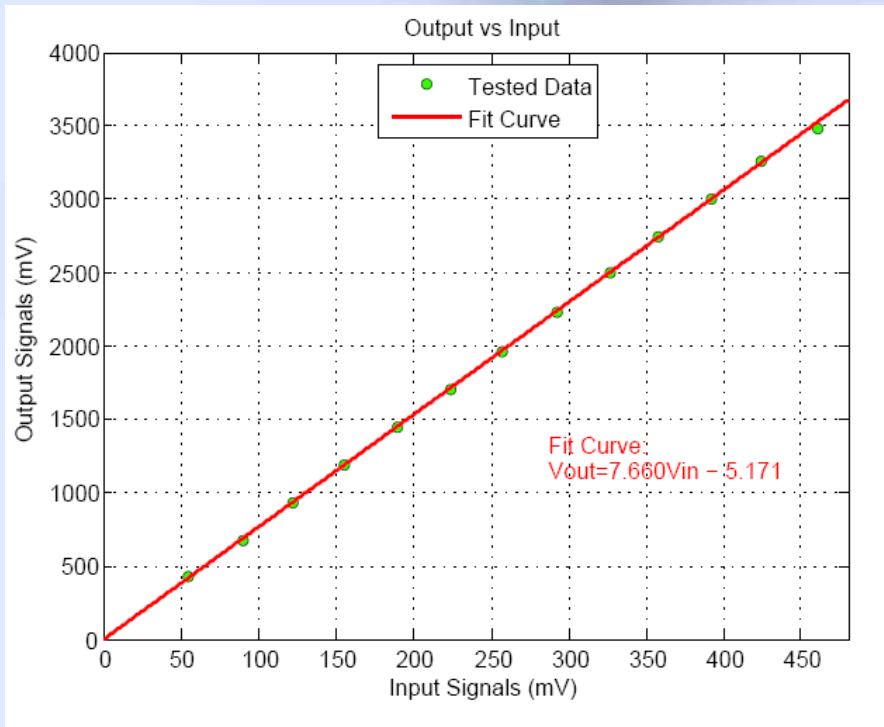


Transfer Characteristic

—— Before Aging Vs. After Aging

Pre-Amp 004#

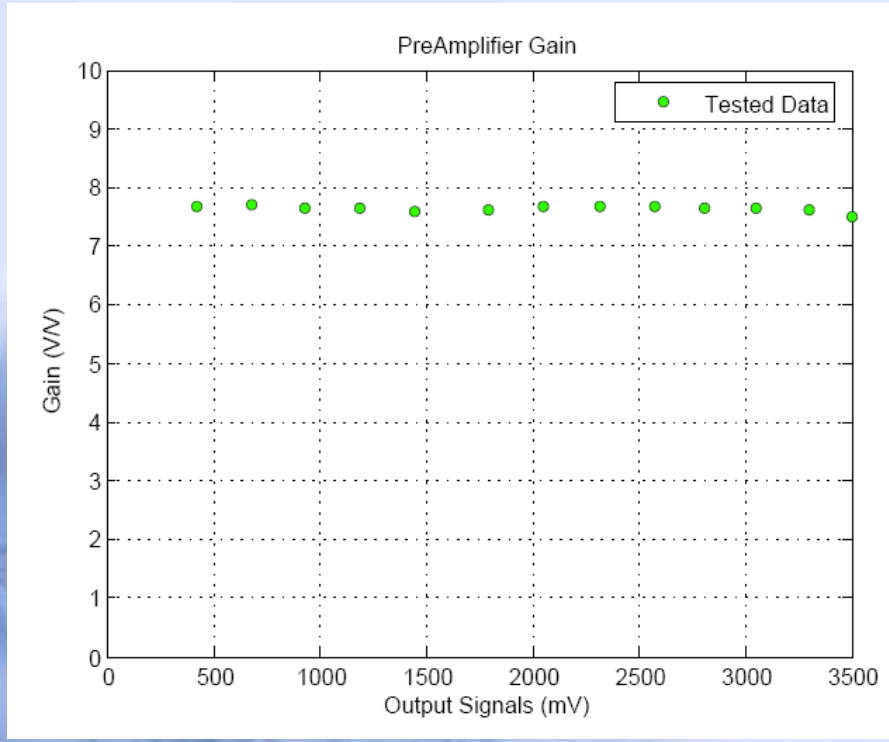


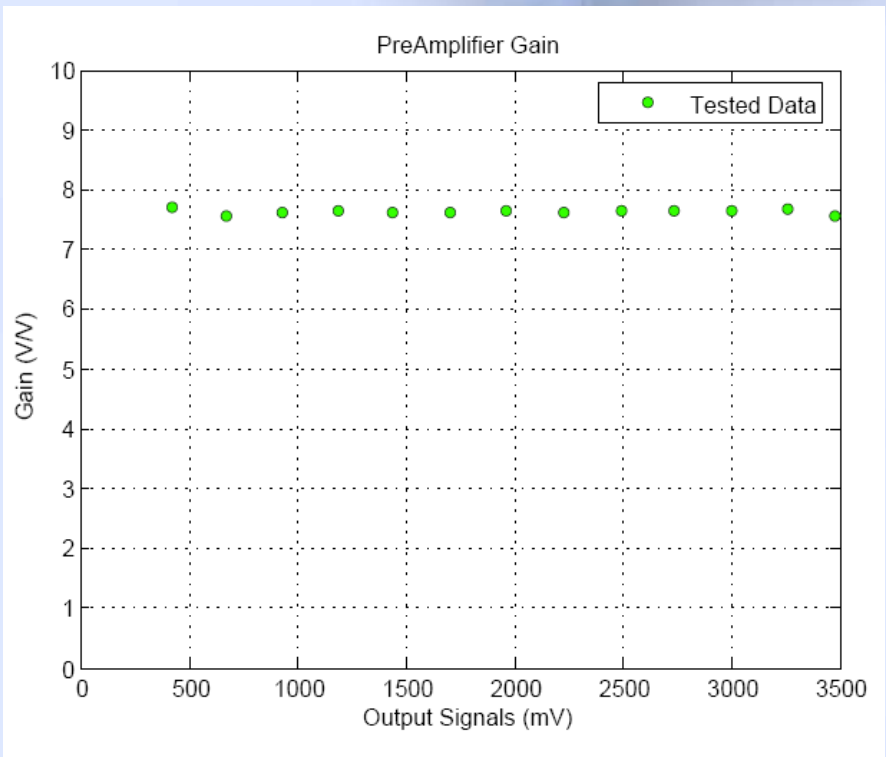


Gain

—— Before Aging Vs. After Aging

Pre-Amp 004#

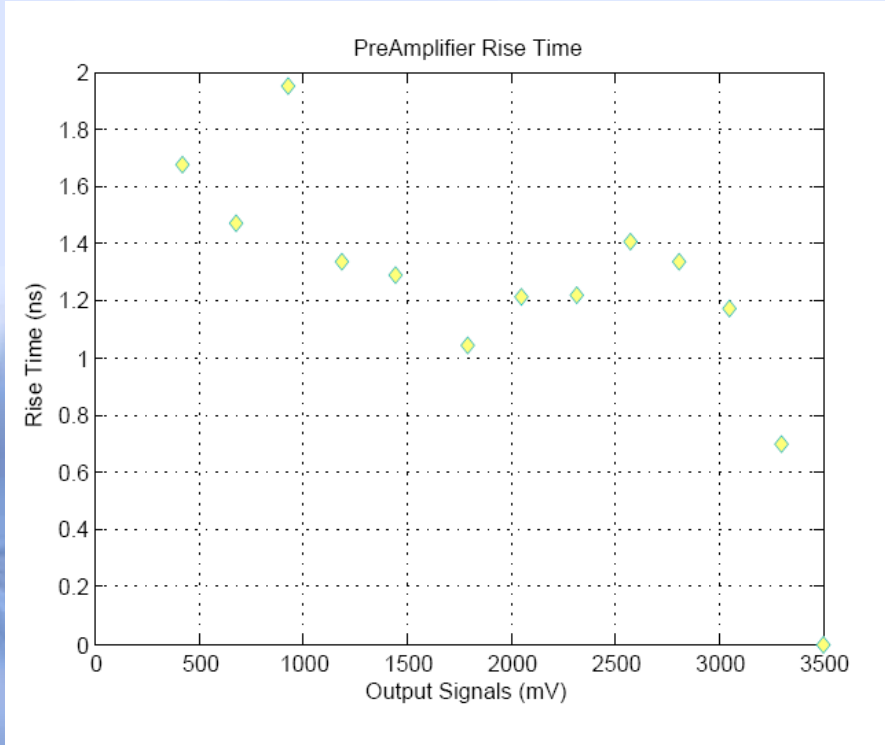


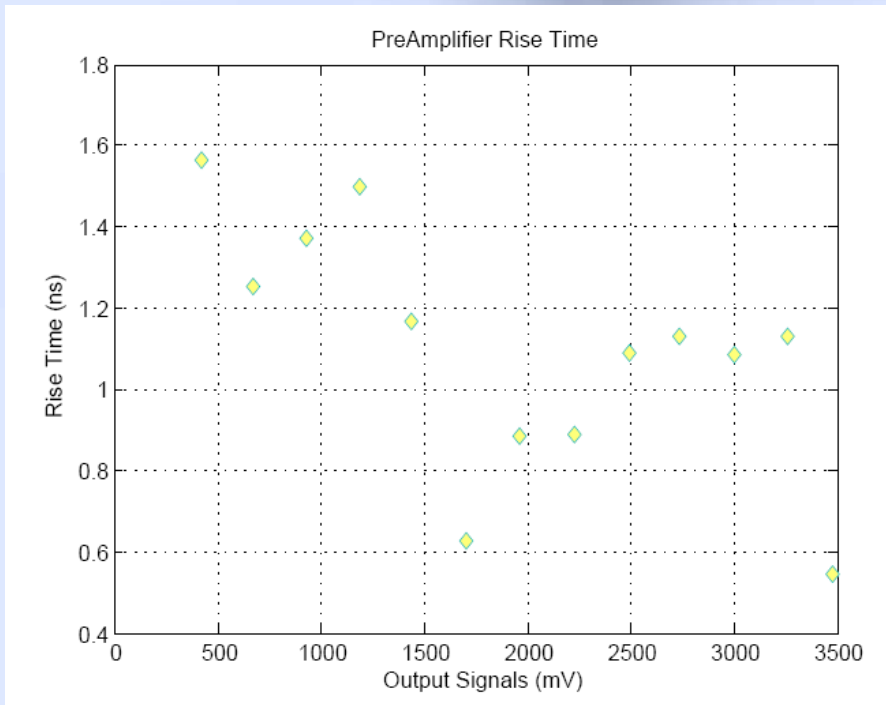


Rise Time

—— Before Aging Vs. After Aging

Pre-Amp 004#

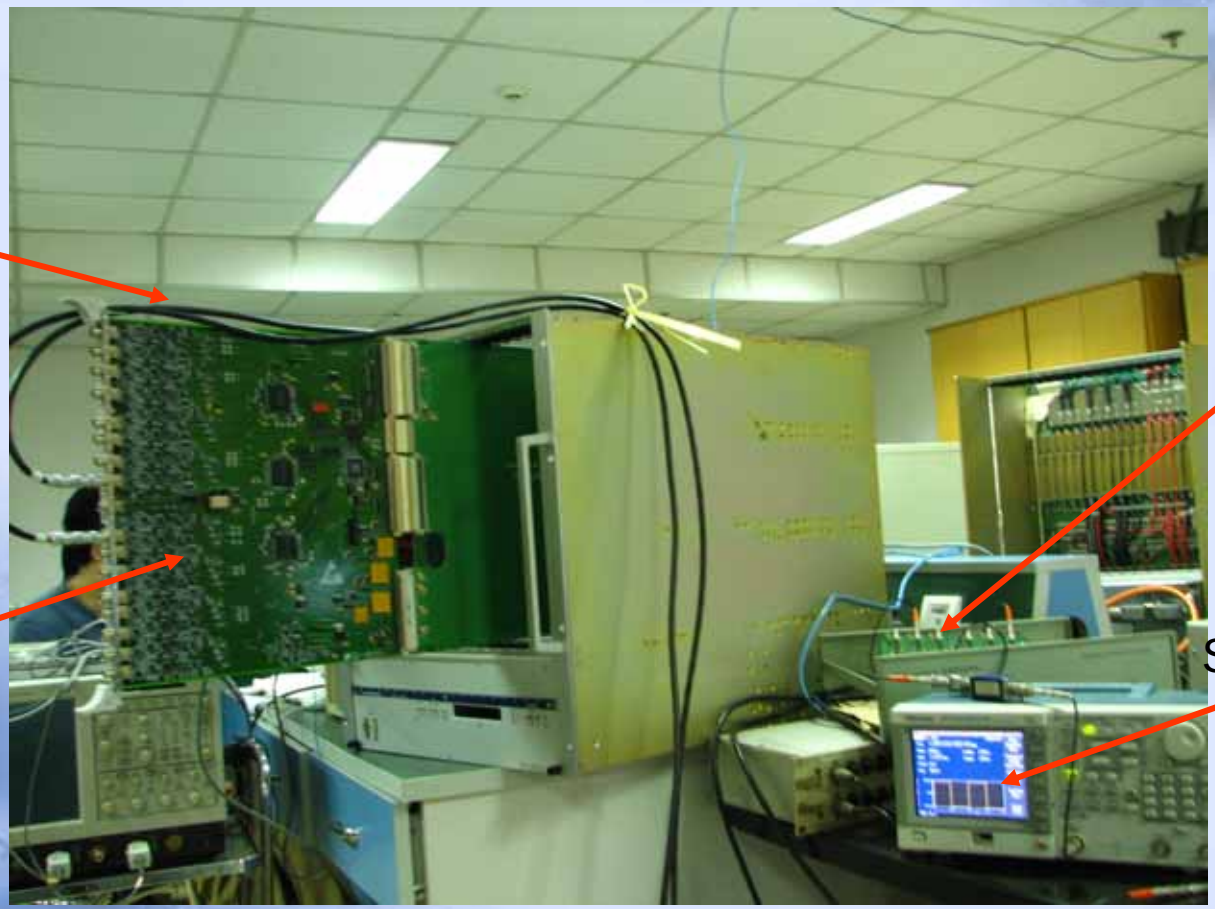




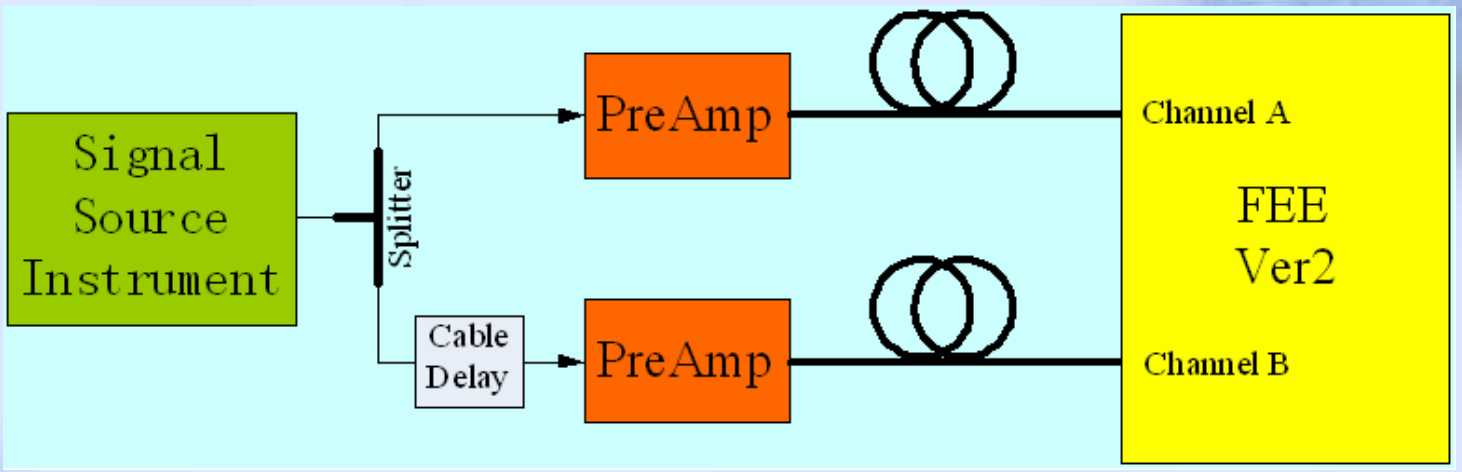
FEE 3.0

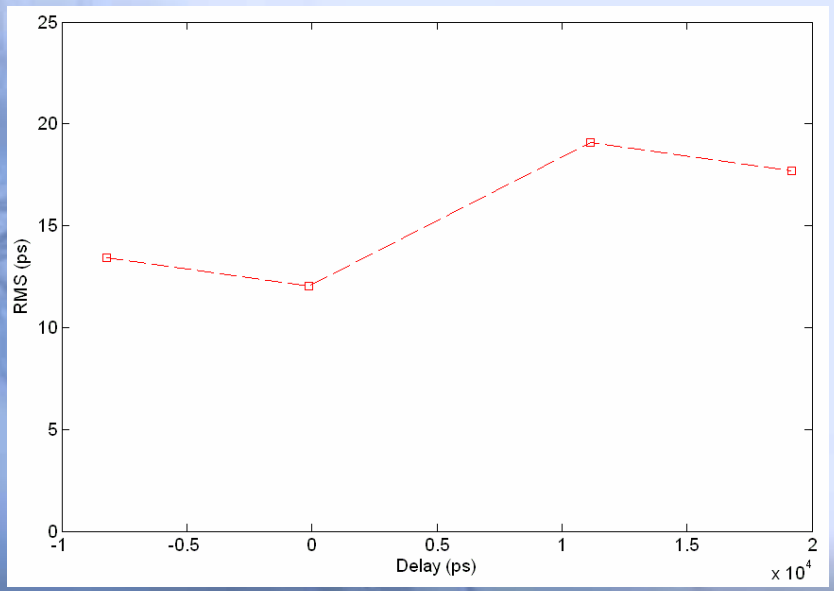
- PCB Layout was finished on March 21, 2006
  - No change in time measurement part
  - The improved Q-T circuit is applied in this version
- The first module is under test since April 6, 2006
  - 2 channels' performance for time and charge measurement were tested
  - All the 16 channels were soldered
    - About 9A current consumed with 5V power supply
  - The small system will be set for test
    - Four FEE 3.0 modules are scheduled to be involved in the system

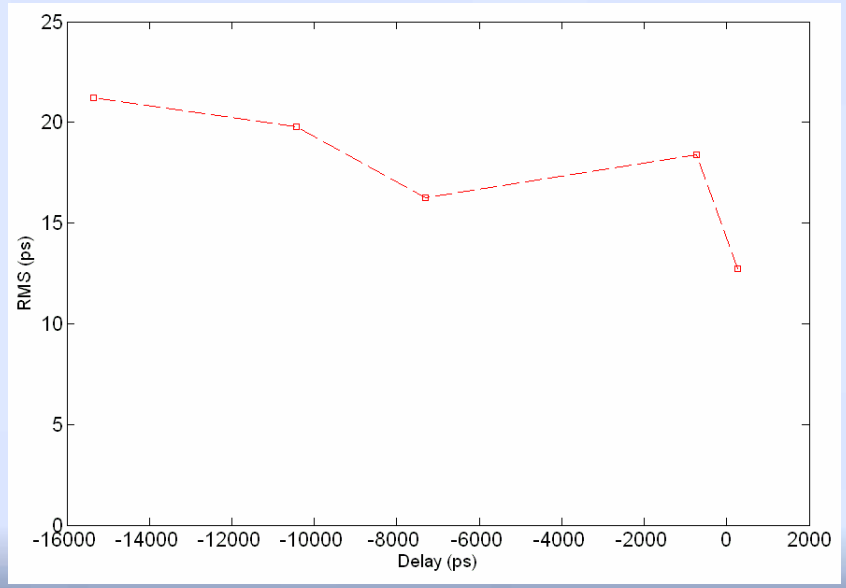
FEE 3.0 Test



Cable Delay Test for FEE 3.0

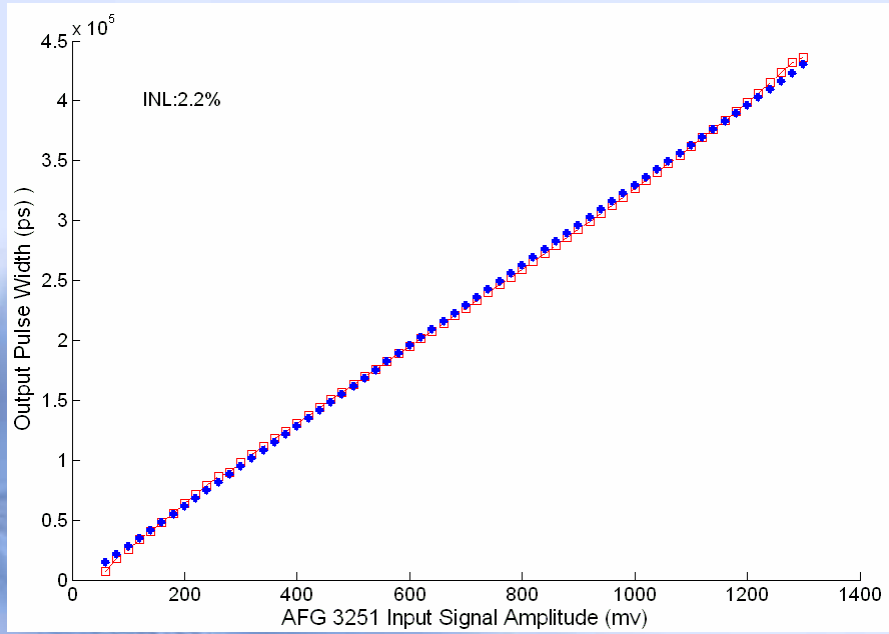




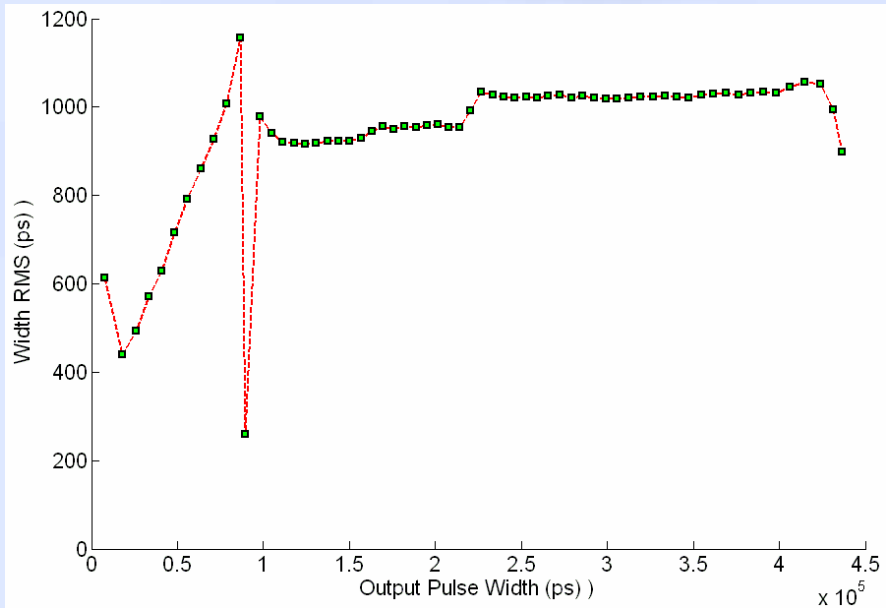


Charge Measurement Test for FEE 3.0 ’s Q-T Circuit

Nonlinearity



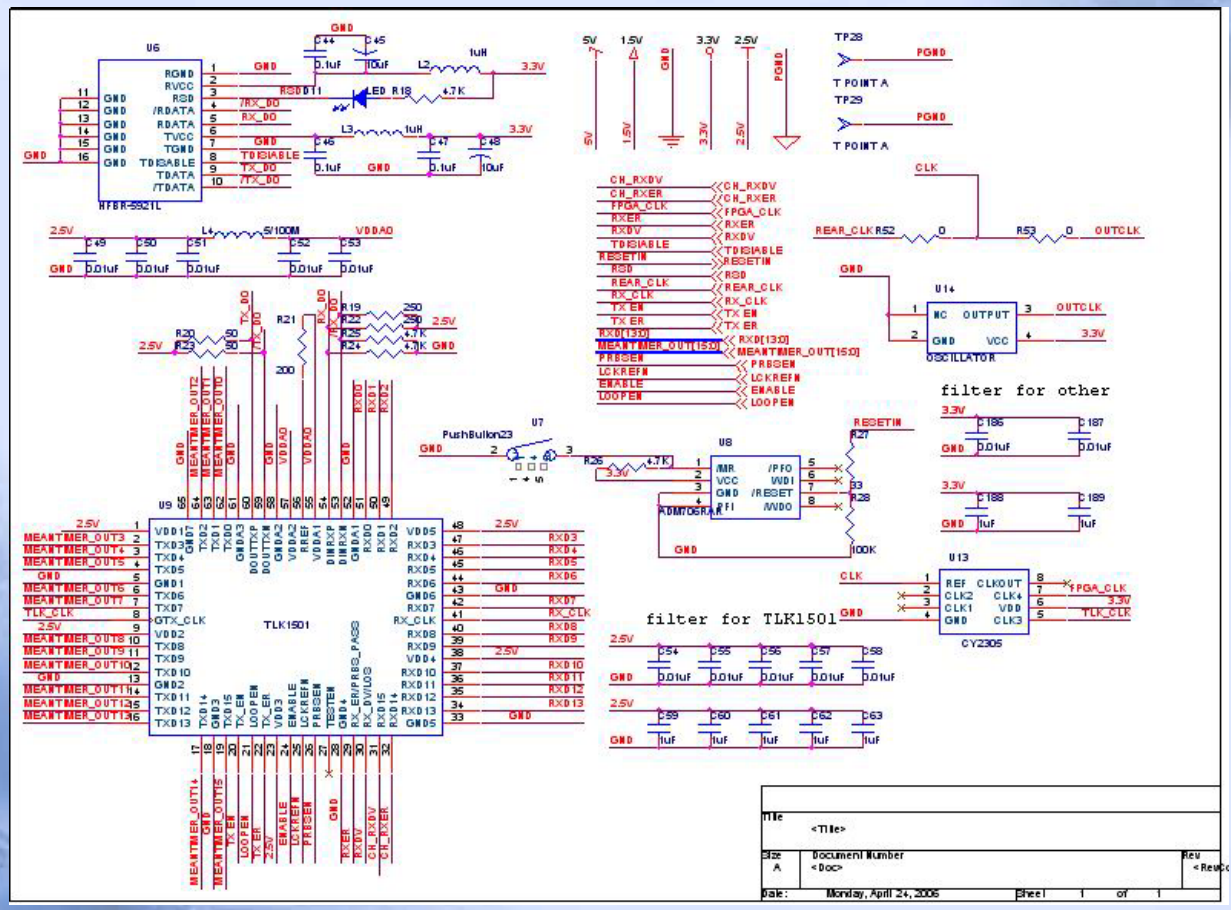
Error



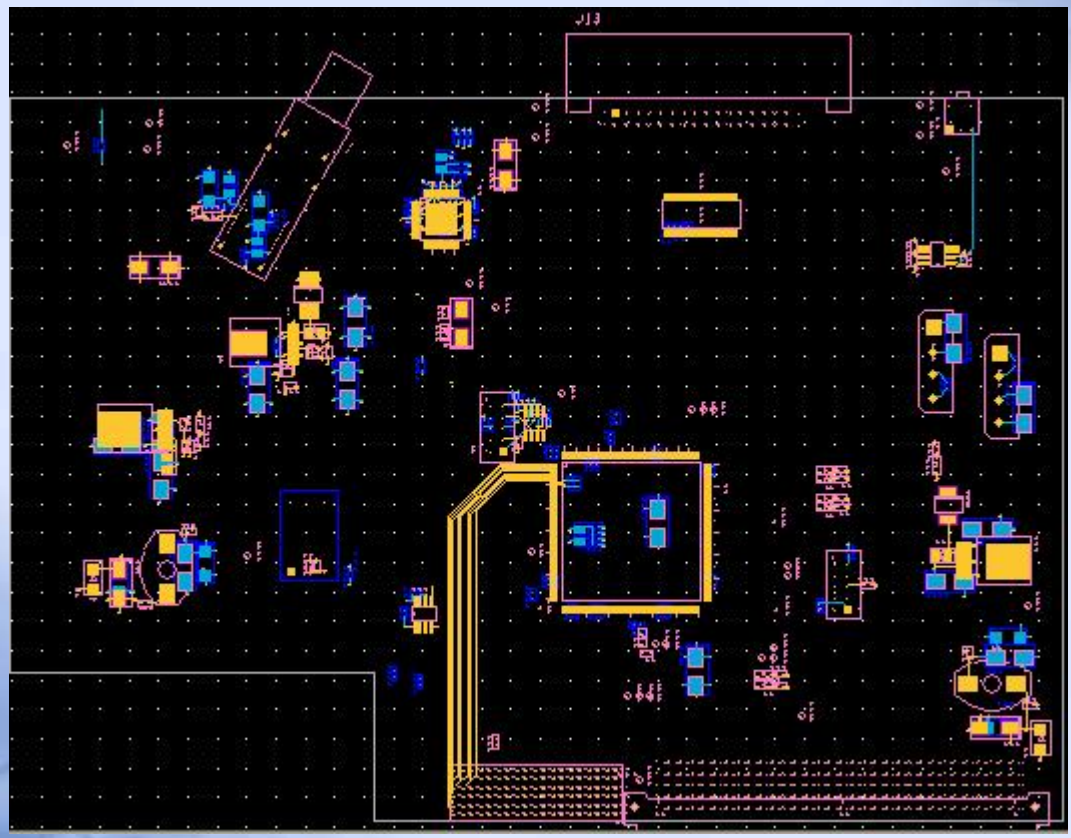
FEE_Rear Module

- The 2nd version has been tested before January, 2006
  - Receiving mean timer signals from FEE
  - Transmitting the signals via fiber after parallel-to-serial conversion
  - Tested with FEE or TOF Trigger Module
- More outputs were requested to be appended
  - In addition to the optical communication with Trigger System, electronical outputs are requested
- New design's PCB layout is in progress
  - Schematic is finished
  - PCB layout is scheduled to be finished before the middle of May, 2006

Schematic of FEE_Rear 3.0



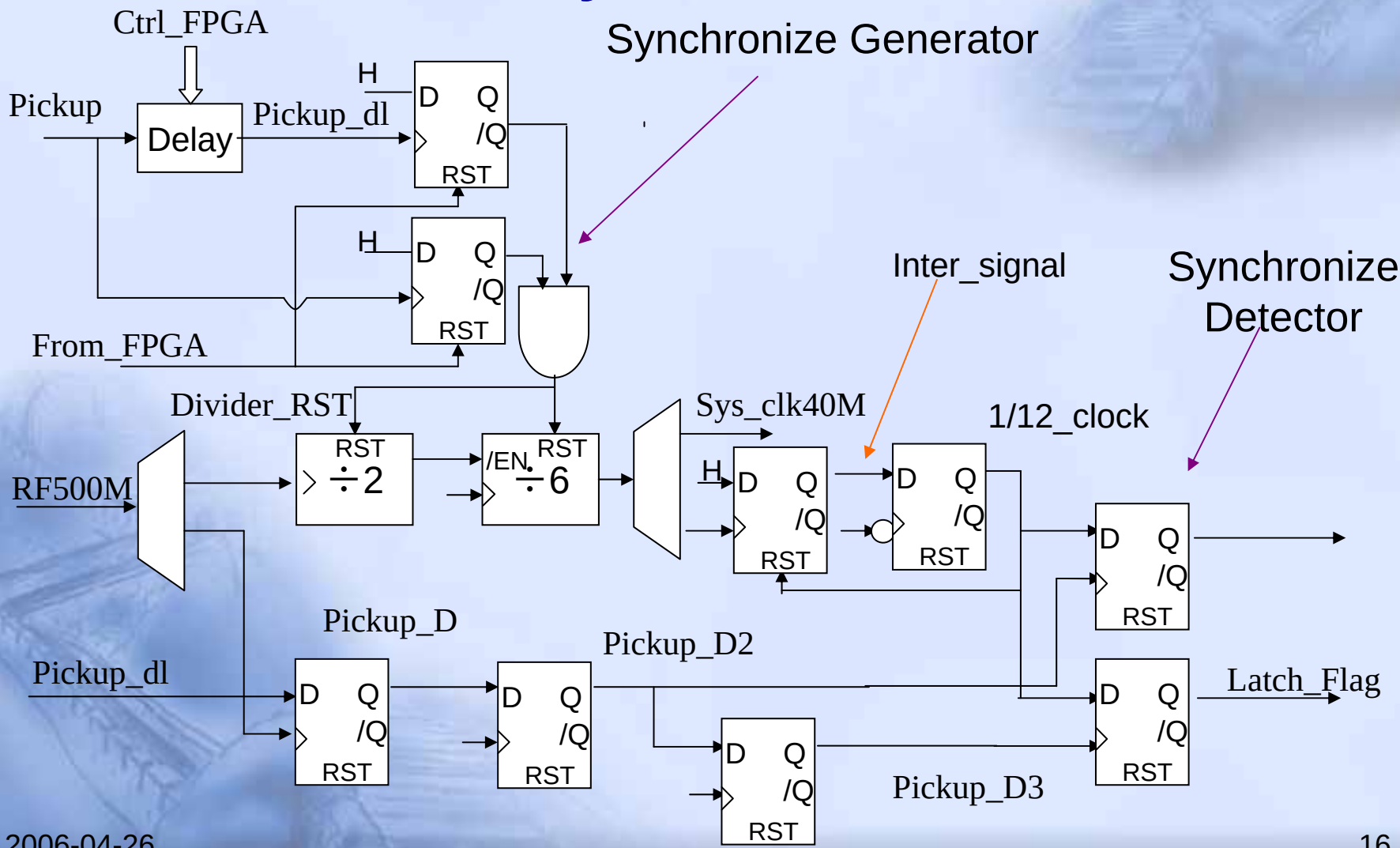
PCB Layout of FEE_Rear 3.0



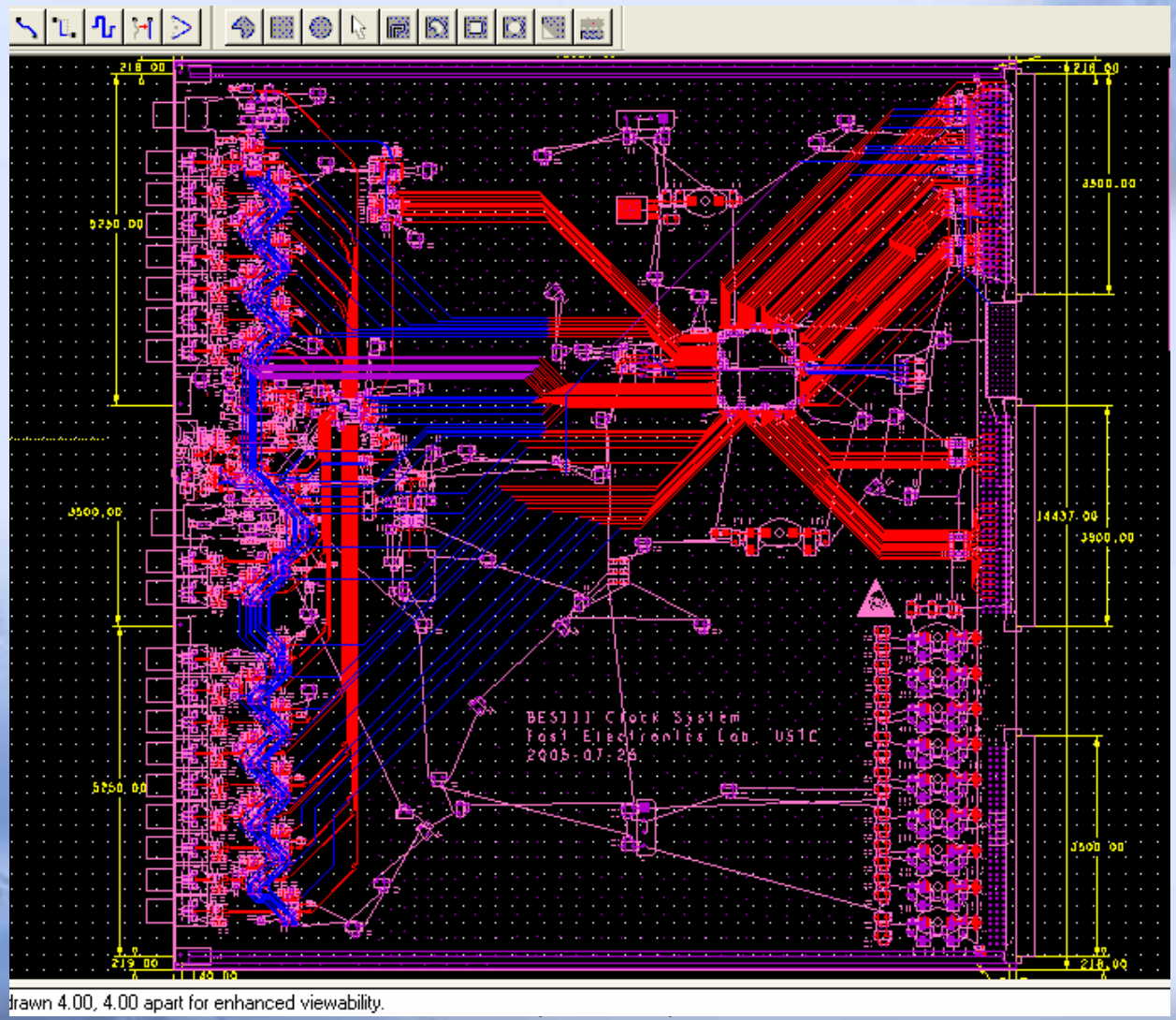
Clock Generator and Fanout Module

- The master module's upgrading is in progress
  - According to the international review, the scheme of synchronization is changed to be implemented with PECL component
  - A flag signal will indicate the synchronization status
  - Schematic was finished
  - PCB layout is scheduled to be finished before May 10, 2006
- The slave module's test is in processing
  - The backup one will be in production

Schematic of Synchronization Circuit



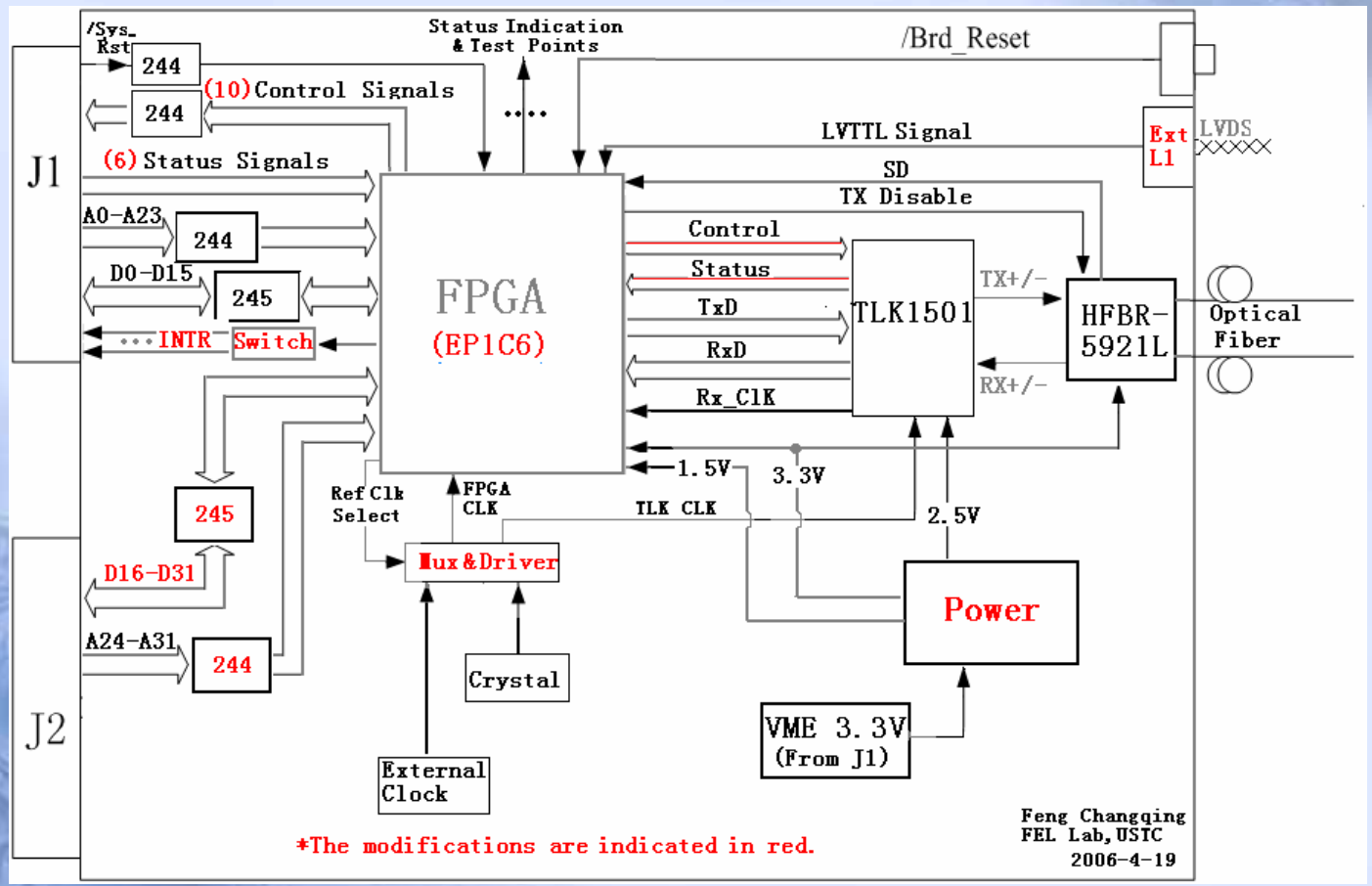
PCB Layout of Clock Generator Module



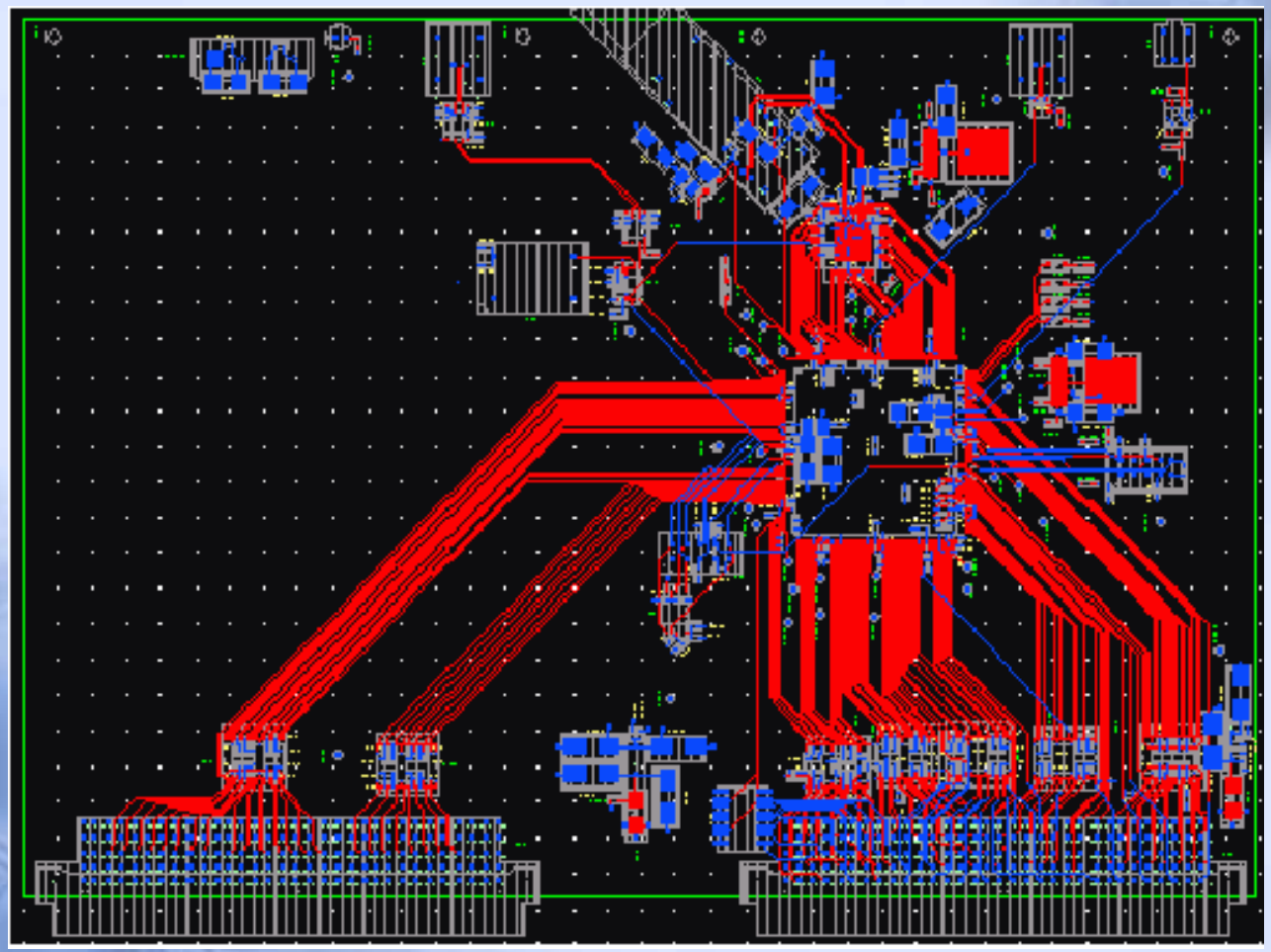
Fast_Control Module

- The 1st version has been tested before October, 2005
  - Control signals fanout function OK
  - Status signals collect function OK
  - Optical signals receiving and transmitting function OK
- More functions was requested to be appended
  - An external L1 signal from TOF Monitor Module should be received
  - A new control signal, FEE-System-Reset, is appended
  - A new status signal, FEE-Config-Done, is appended
- New design's PCB layout is finished
  - Scheduled to be tested before July, 2006

Scheme of Fast_Control 2.0



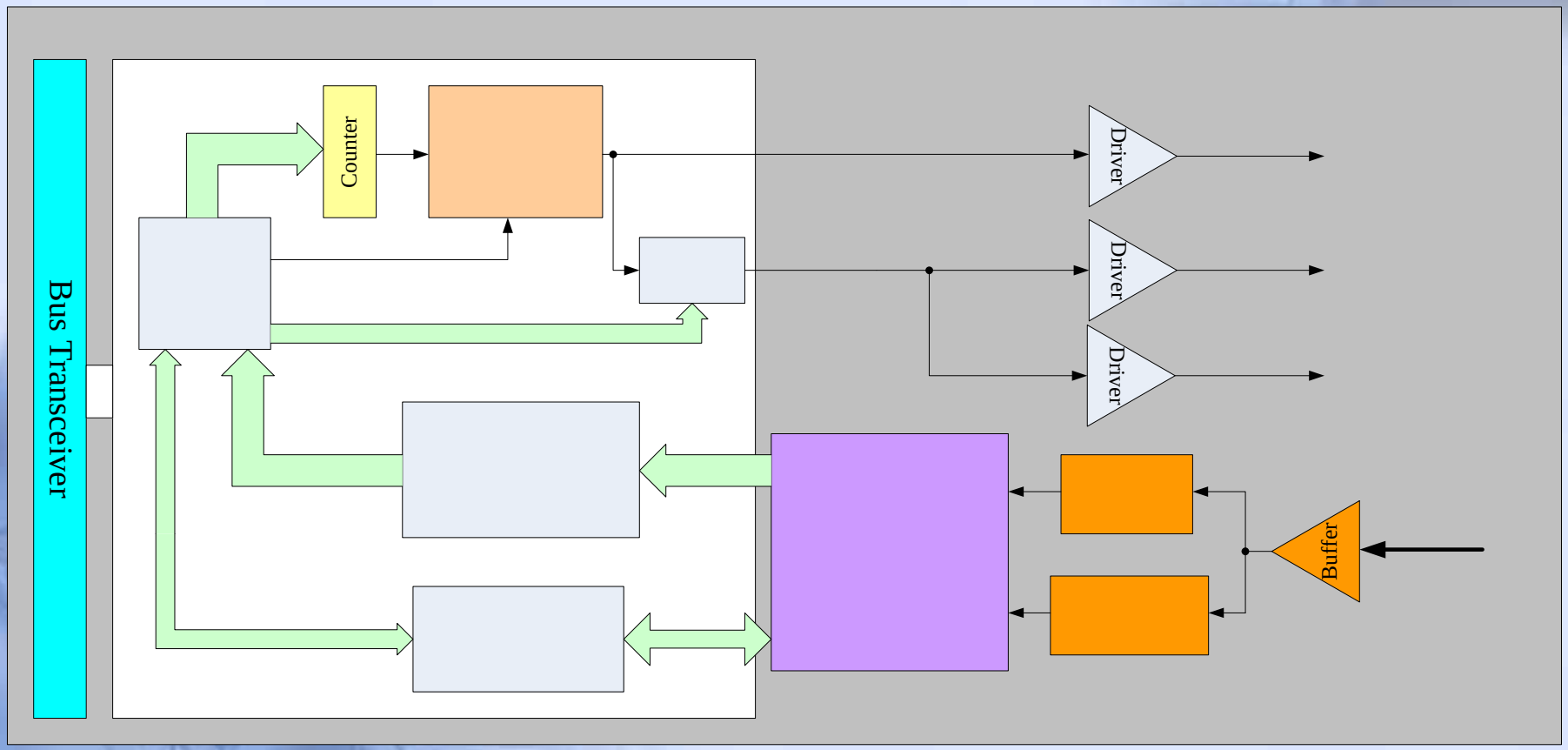
PCB Layout of Fast_Control 2.0



TOF Monitor Control&Readout Module

- Work with the TOF Monitor System
  - Received commands from DAQ
  - Giving signals to Monitor System to let LED or laser produce light
  - Giving “Monitor Trigger” signals to Fast_Control Module to substitute for L1 trigger
- Design is scheduled to begin in July, 2006

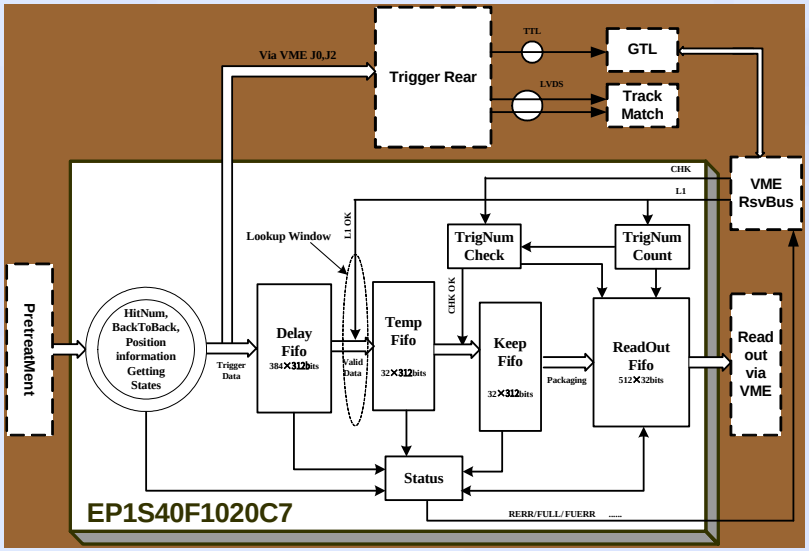
Scheme of Monitor Control&Readout Module



TOF Trigger Module

- Logic for trigger arithmetic is finished
- Logic tested in several ways
  - Test in the online-check mode
  - Test with the FEE_Rear Module
  - Test with the Trigger_Rear Module
  - Test in the simulator system
    - TOF Trigger Module
    - 2 Fast_Control Modules
      - Act as FEE_Rear Modules
    - Trigger_Rear Module
    - Clock Fanout Module
- Test with GTL and tracking match system is on schedule
- Short board version is in consideration

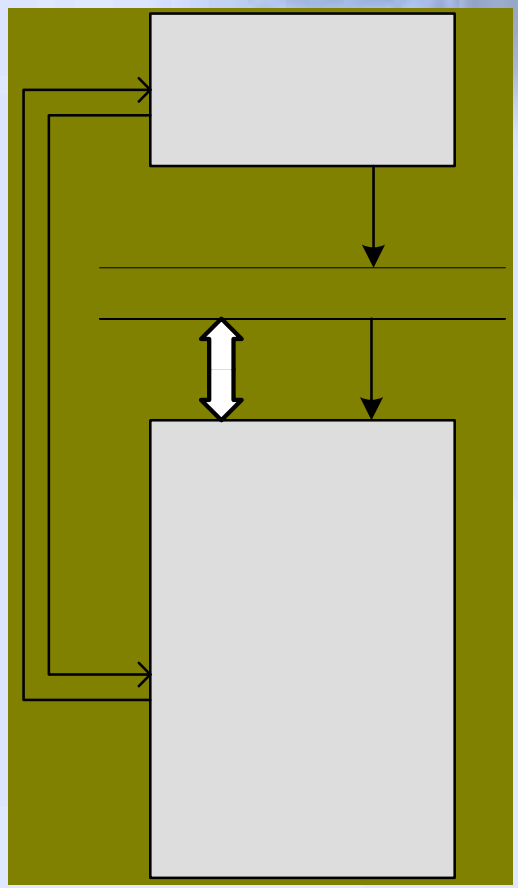
Test in the Online Check Mode



- PretreatMent function
  - OK
- Hitnum/BacktoBack/Position information production
  - OK
- CBLT readout function
  - OK

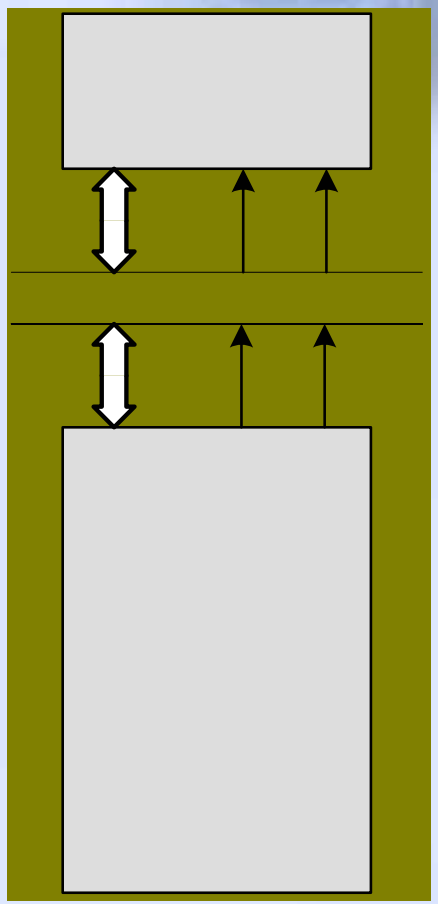
Test with the FEE_Rear Module

- Data transfer function
  - OK
- PretreatMent function
  - OK
- Hitnum/Position information production
  - OK
- CBLT readout function
  - OK

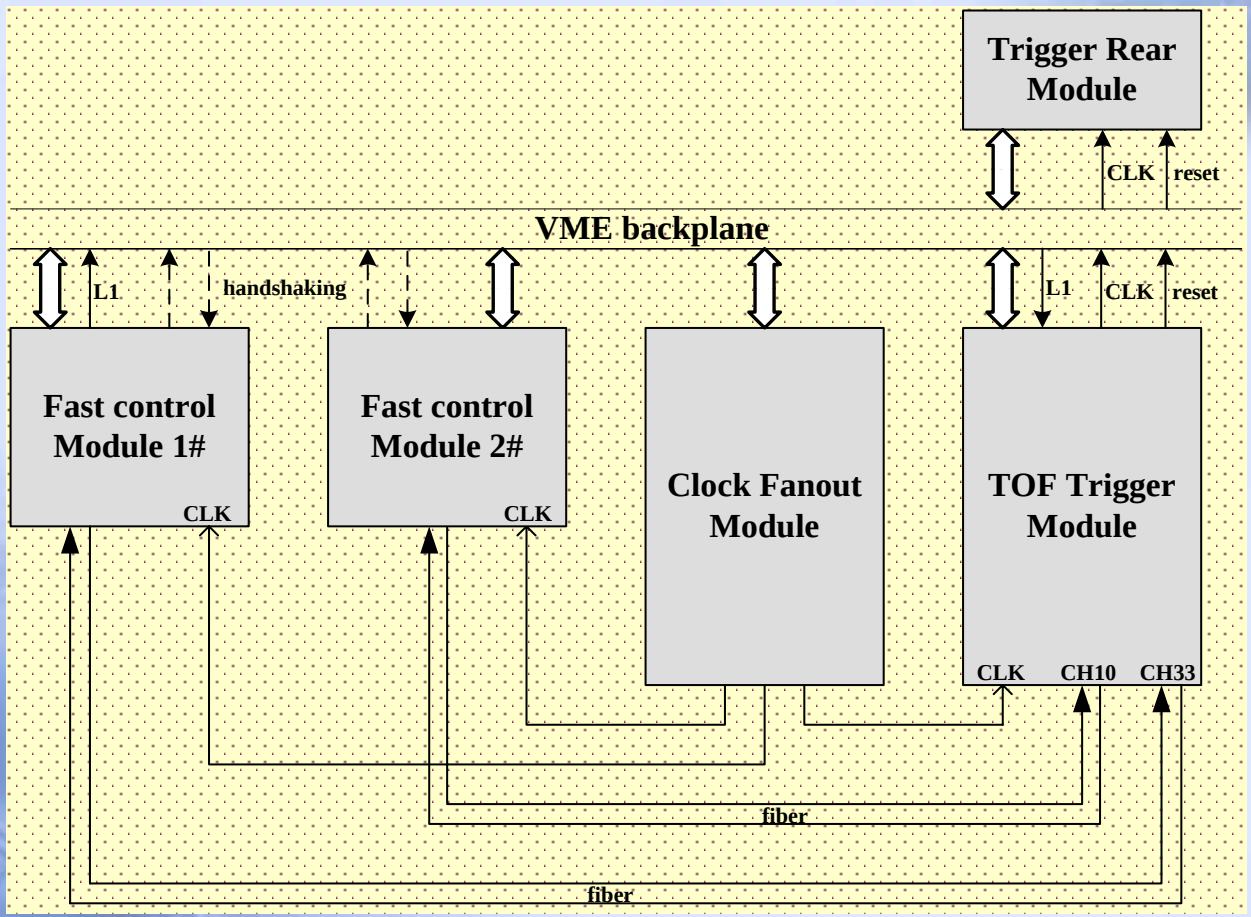


Test with the Trigger_Rear Module

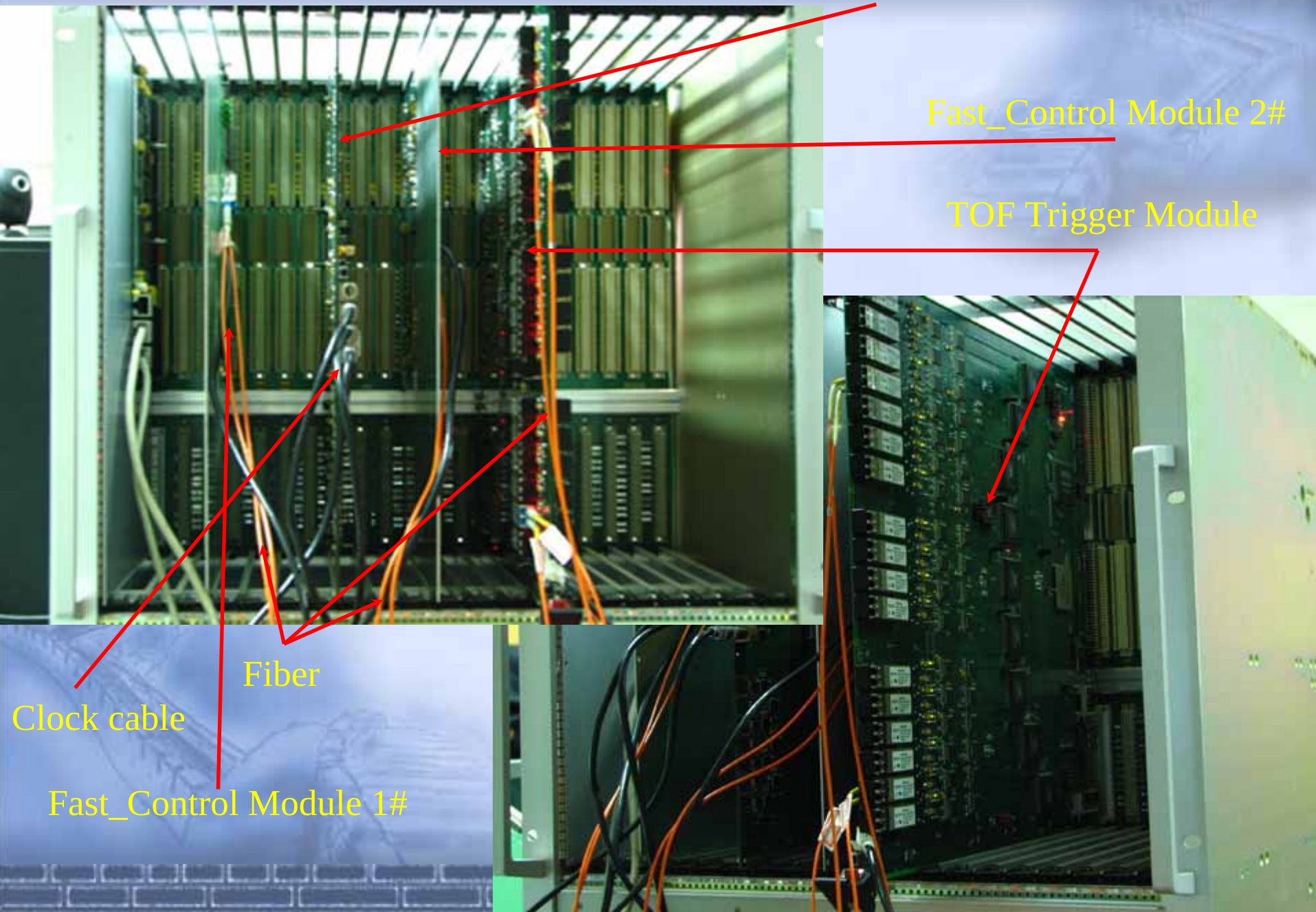
- Data transmission via VME J0/P0 and J2/P2
  - OK
- Logic of Trigger Rear
  - OK
- Serializers and drivers on the Trigger_Rear Module
  - Works well

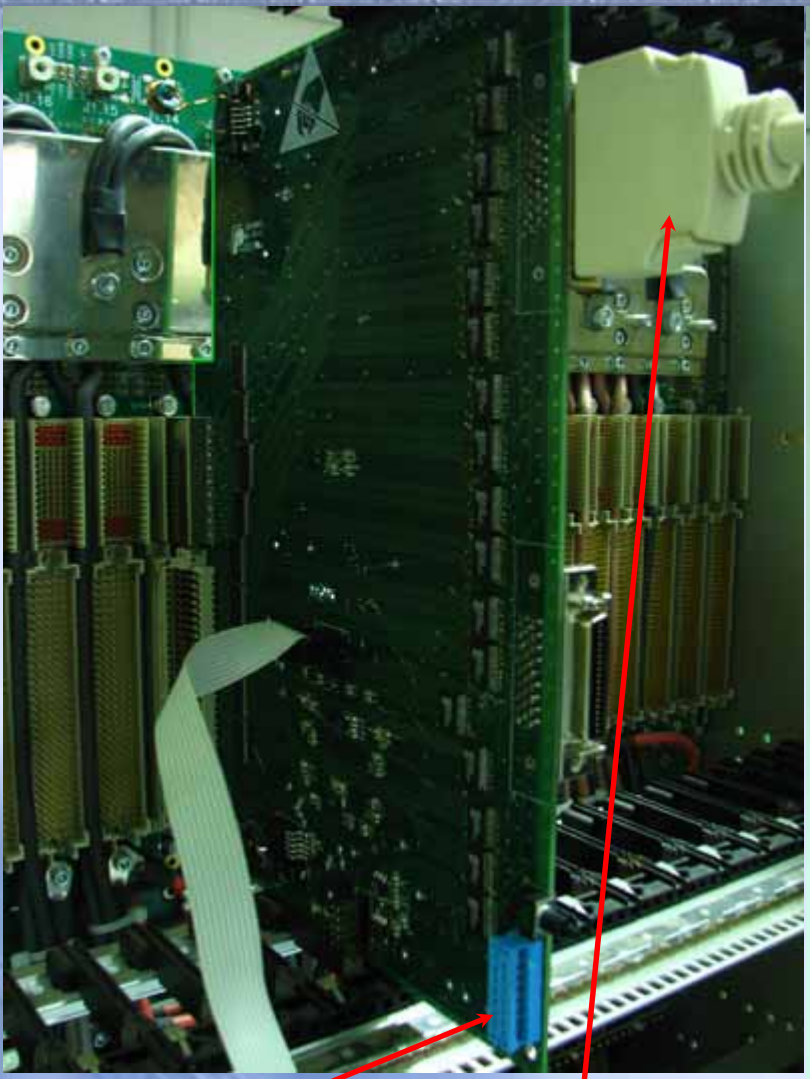


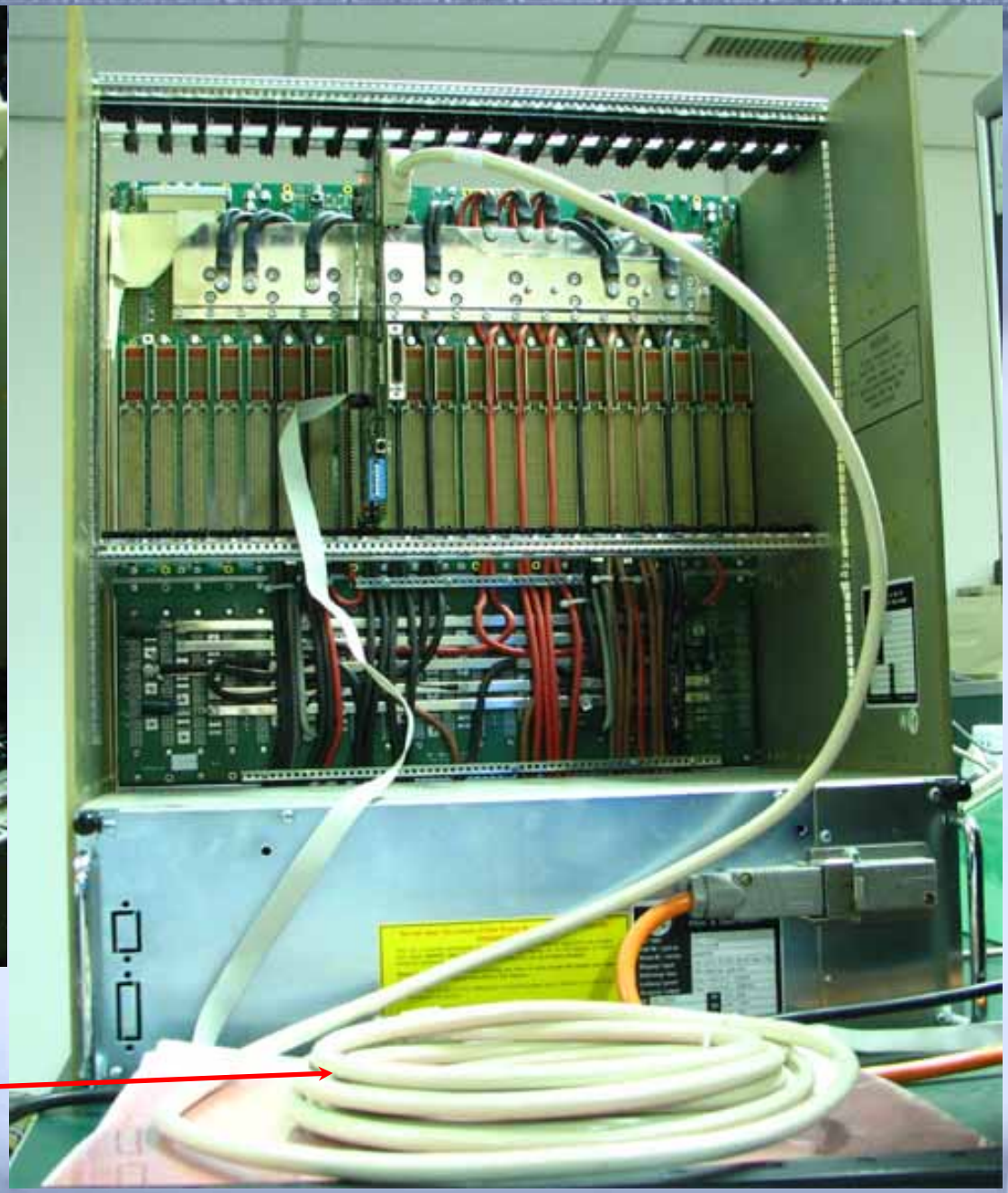
Test in the simulator system



Pictures of the Simulator System







To GTL

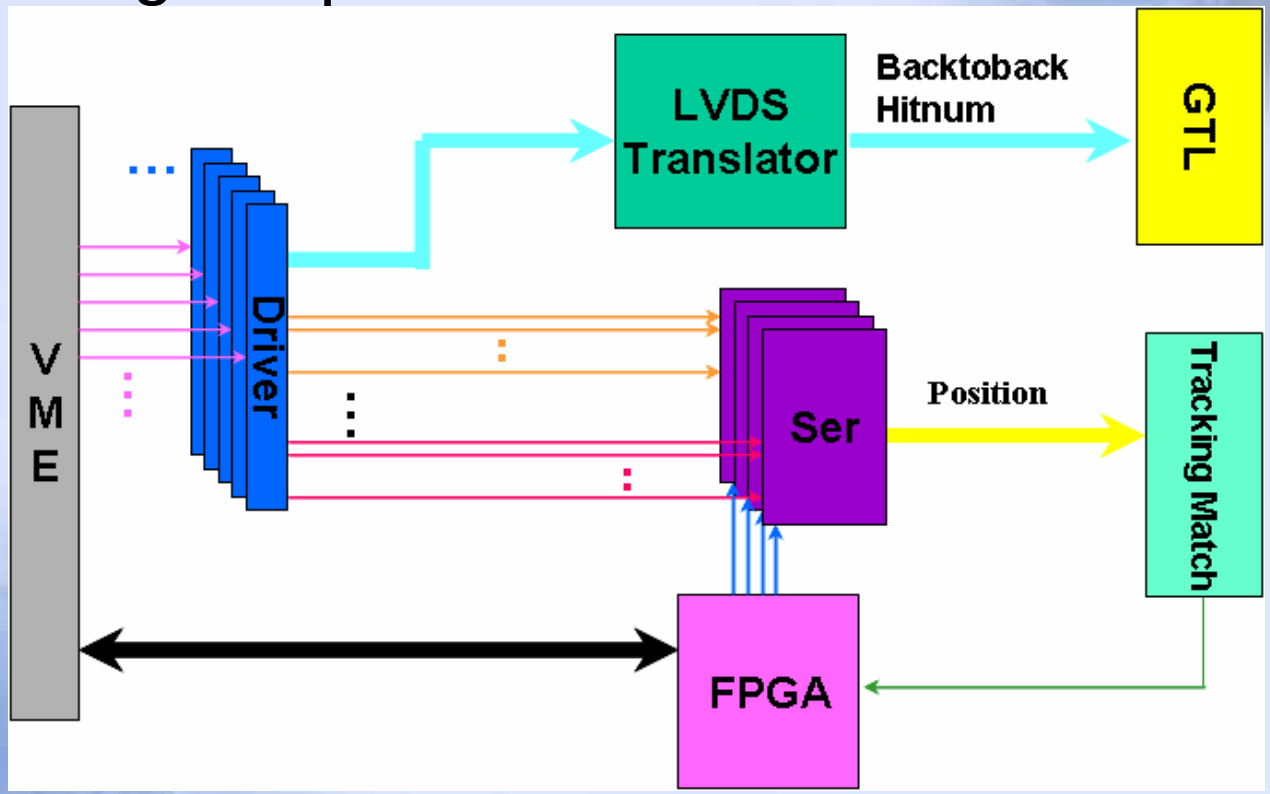
5m Differential cable
to Tracking Match System

Test in the simulator system

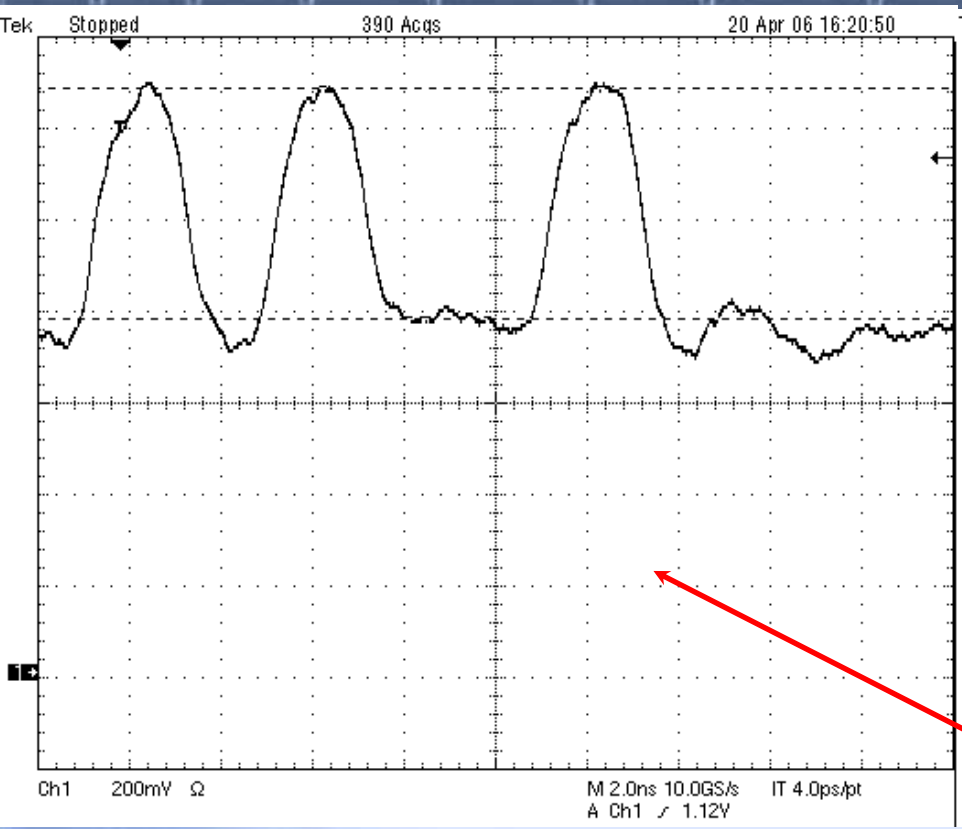
- Fiber transfer function
  - OK
- PretreatMent function
  - OK
- Hitnum/BacktoBack/Position information production
  - OK
- CBLT readout function
  - OK
- Data transfer via VME J0 and J2
  - OK
- Logic of Trigger_Rear
  - OK
- Serializers and drivers on the Trigger_Rear Module
  - Works well

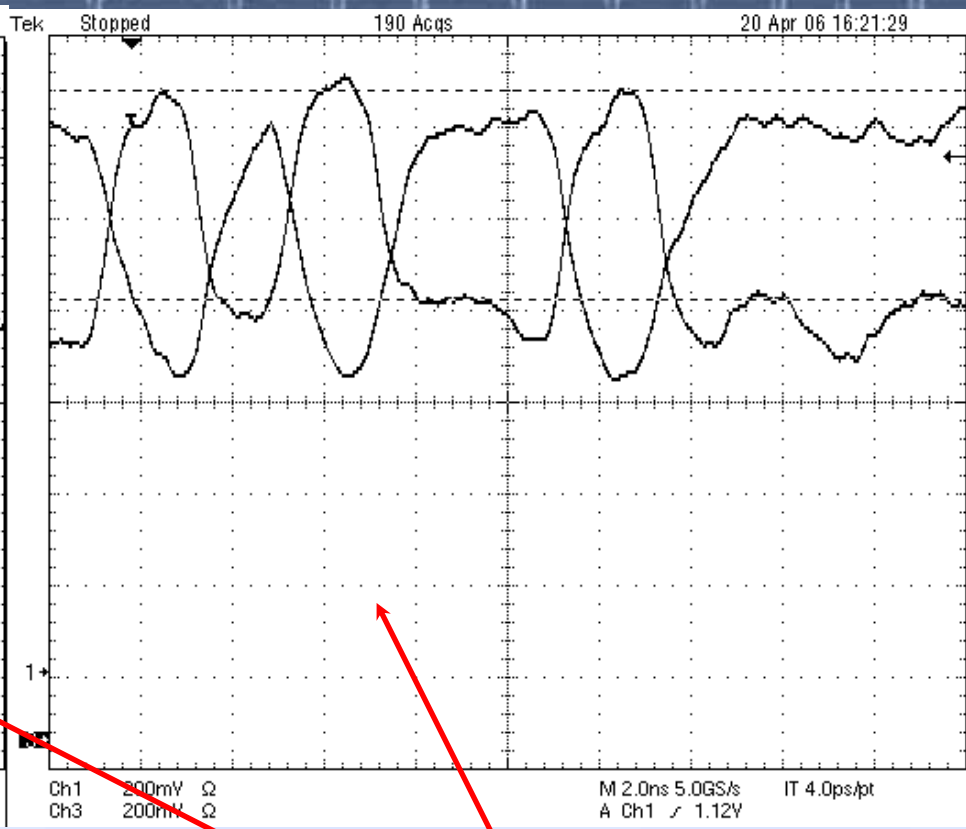
Trigger_Rear Module

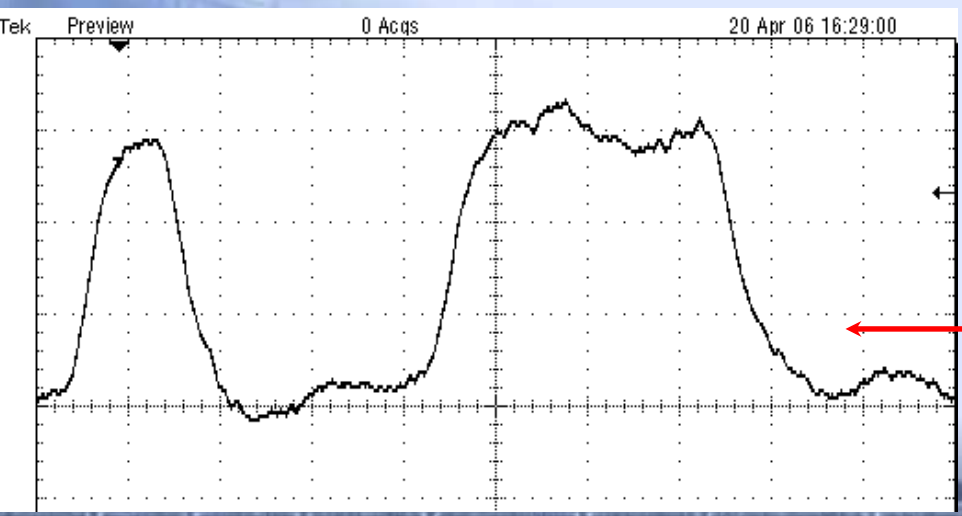
- Transmitting the position/hitnum/backtoback signals



- PCB production was finished on February 23, 2006







0100100000

0001110000

Outputs of LV1023

Thanks!