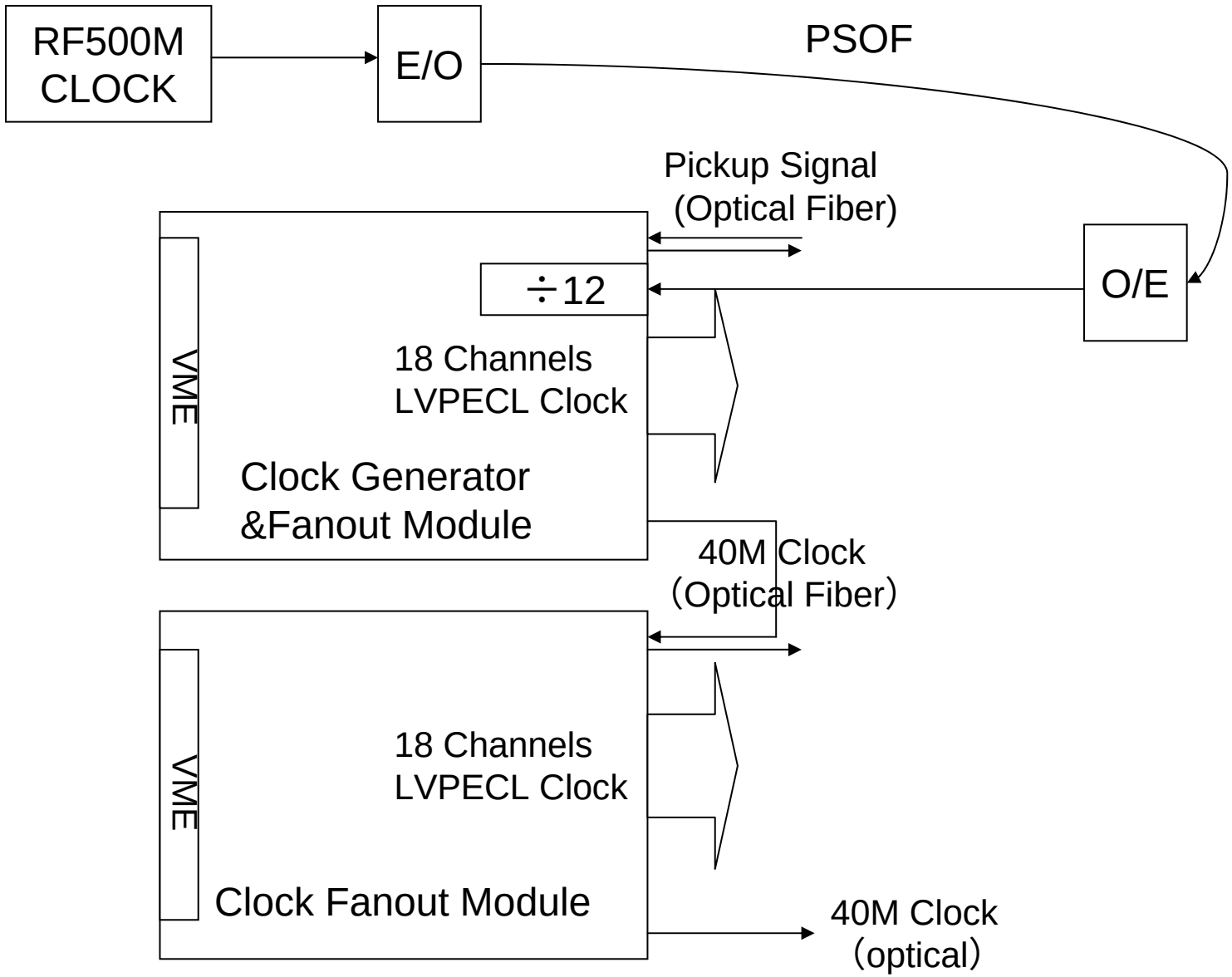
Improved Design For BESIII Clock Generator Module

Li Hao

2006.04.27

Diagram of BESIII Clock System



Function of the Clock G&F Module

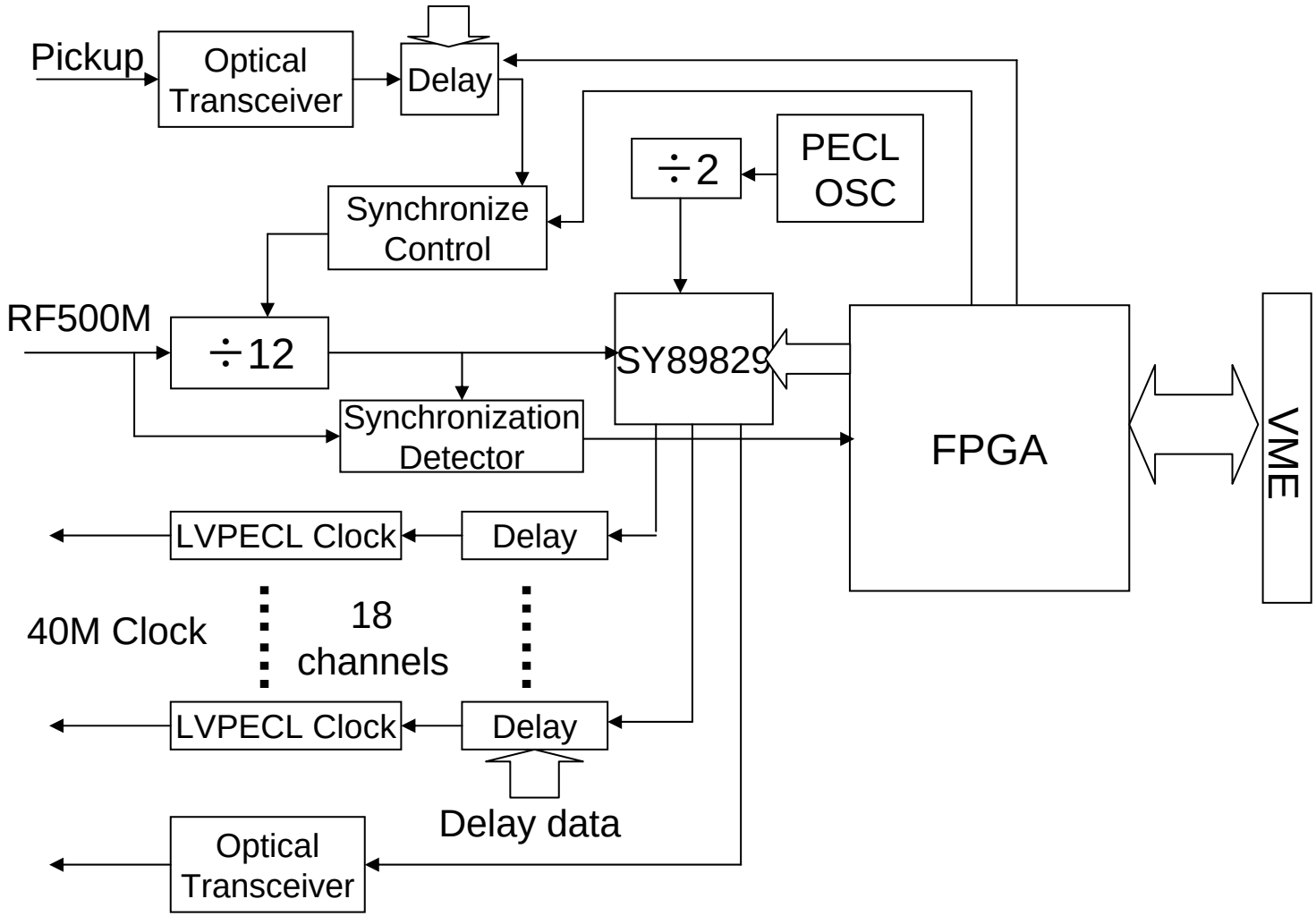
Master module (clock generator & fanout module)

1. Receive system clock (499.8MHz RF signal) and Pickup signal.
2. Generate 41.65MHz clock from RF clock , synchronized with the rising edge of Pickup signal.
3. 1:20 Fanout (18 Diff LVPECL and 2 Optical outputs)

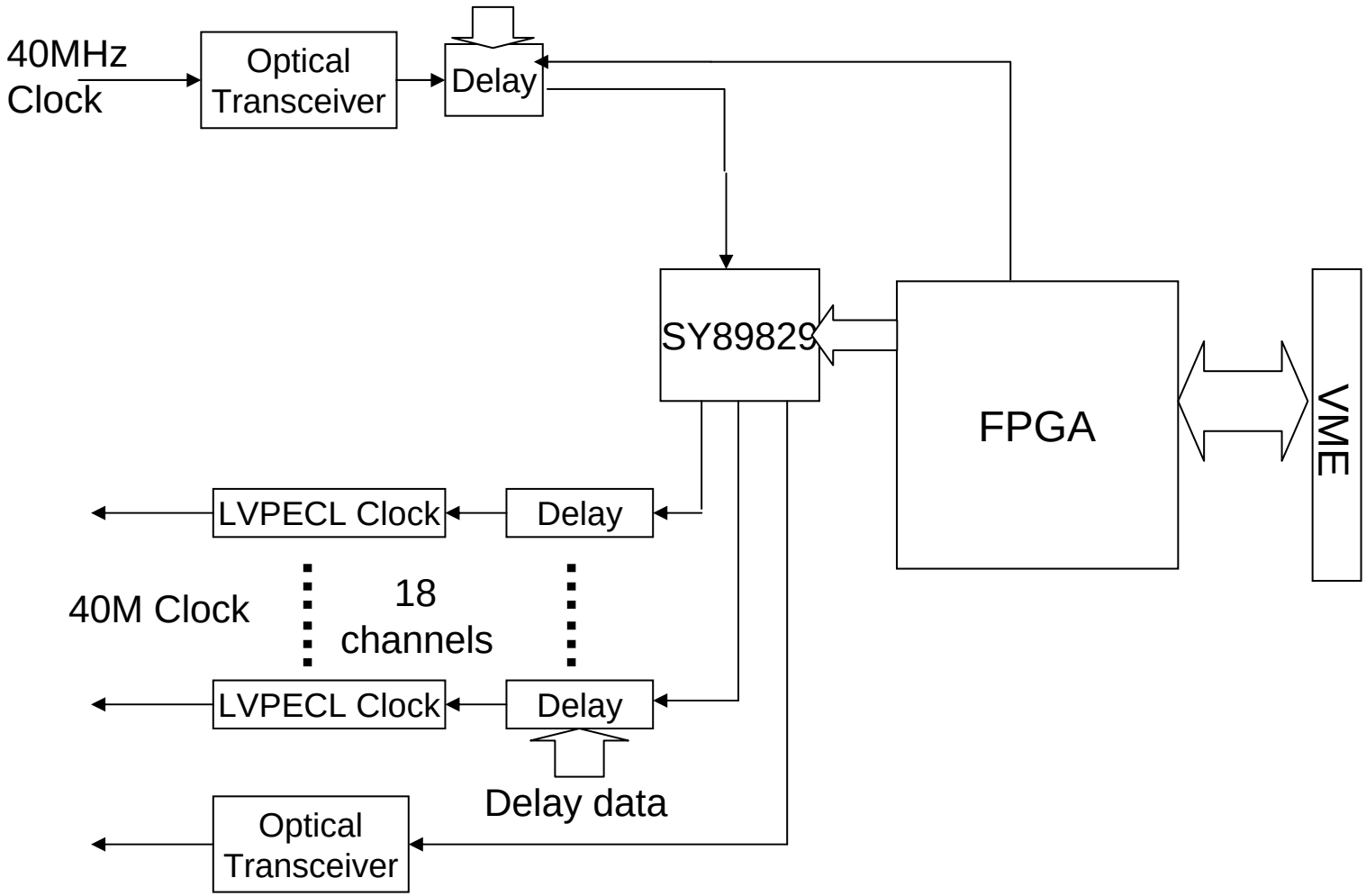
Slave module (clock fanout module)

1. Receive 41.65MHz clock from clock G&F module.
2. 1:20 Fanout (18 Diff LVPECL and 2 Optical outputs)

Scheme of Clock G&F Module



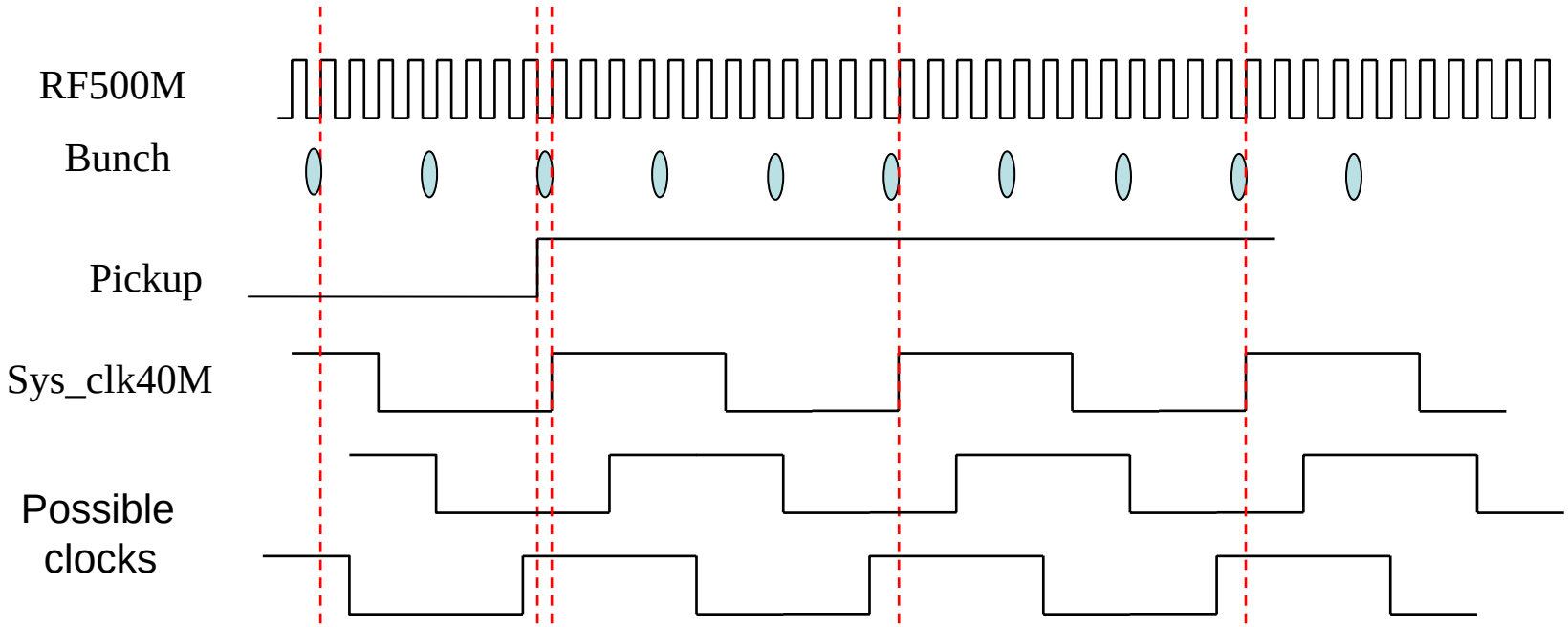
Scheme of Clock Fanout Module



Improvement on new G&F Module

1. According to the advice of international review, the clock divider's synchronization logic will be implemented with ECLinPS devices, rather than FPGA
2. A flag is appended for synchronization status indication.
3. According to VME64 XP specification, modify FPGA's logic.

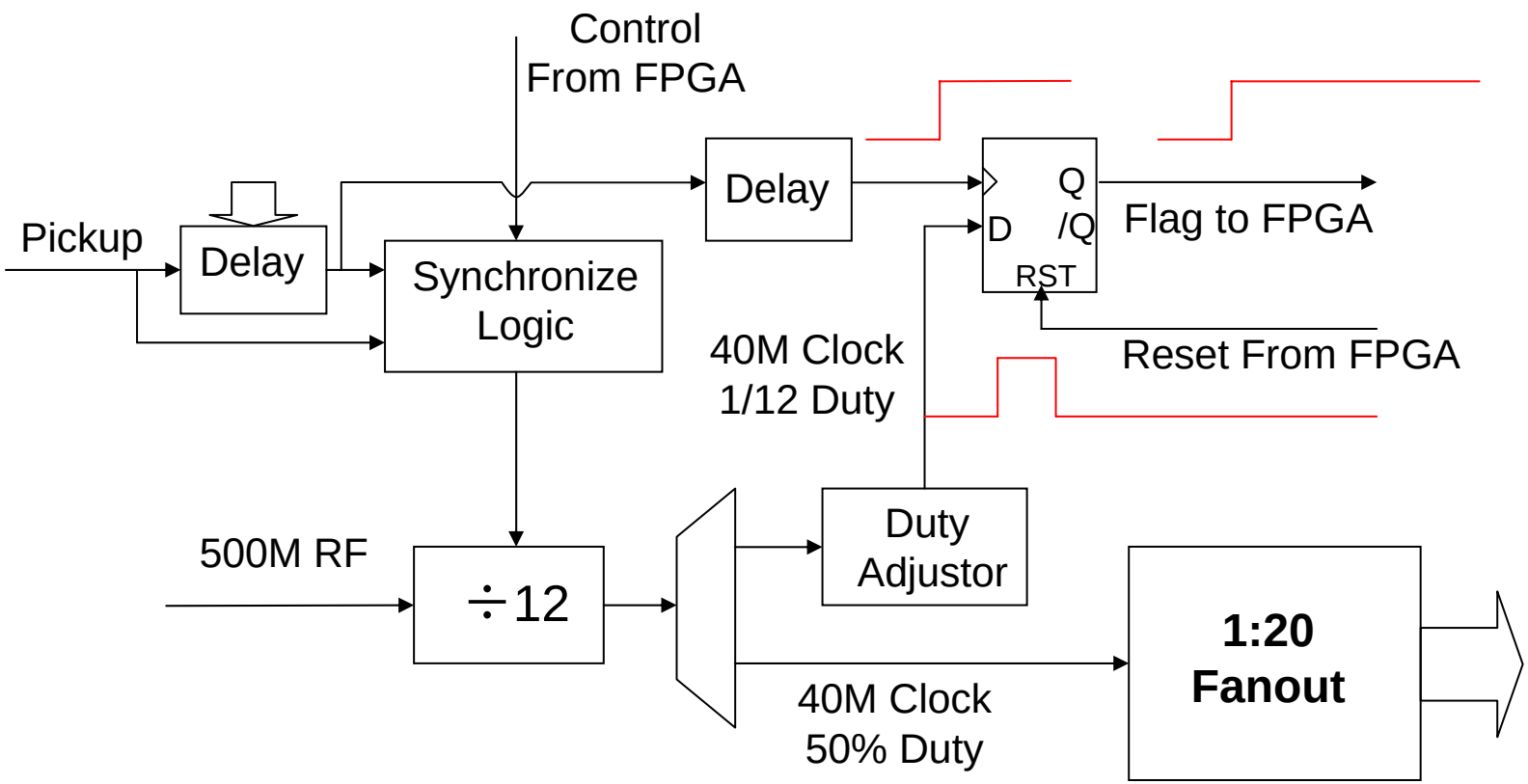
What does ‘Synchronize’ mean?



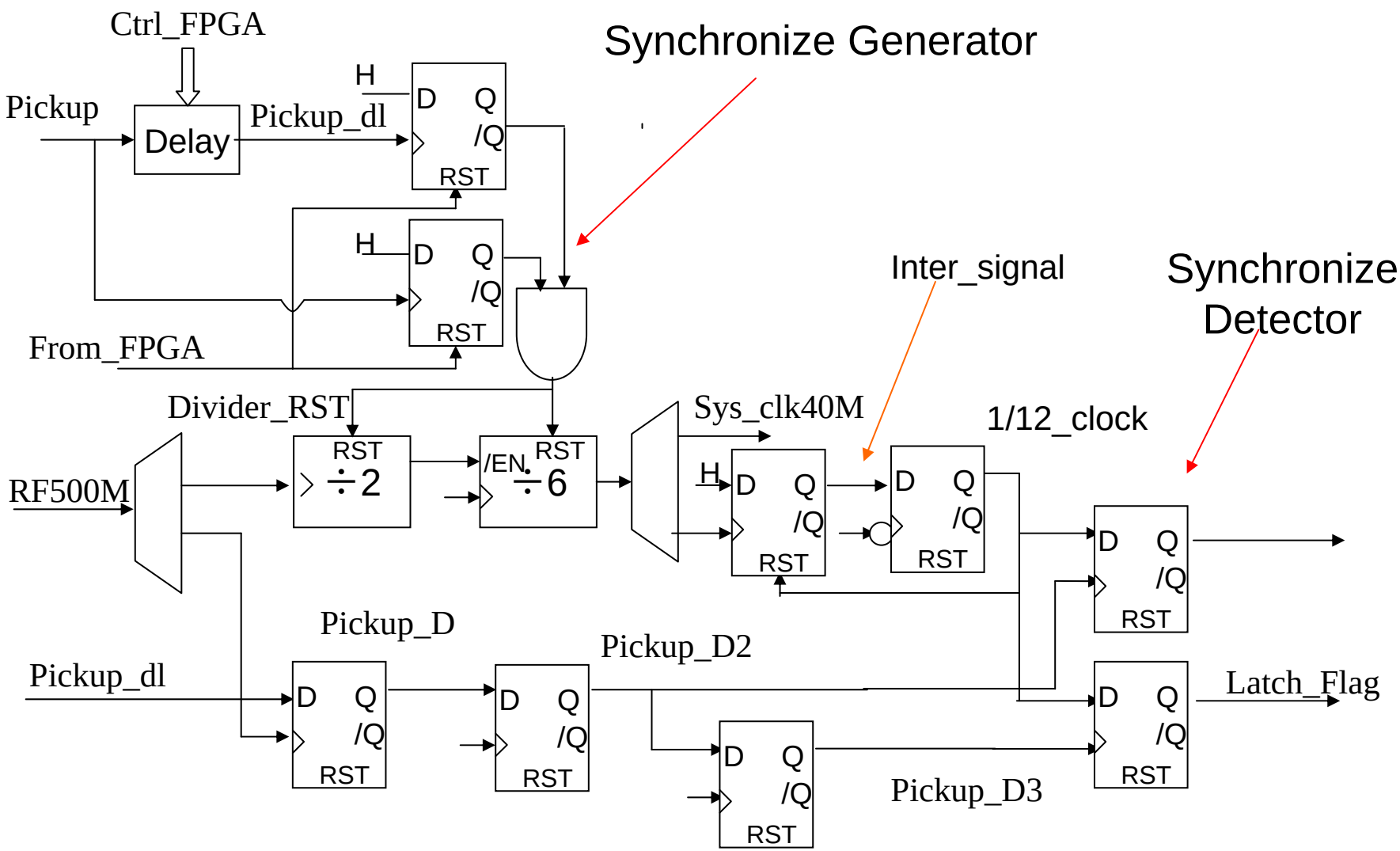
One bunch comes every 4 RF clock cycles.

There are 12 possible clocks if no Synchronization

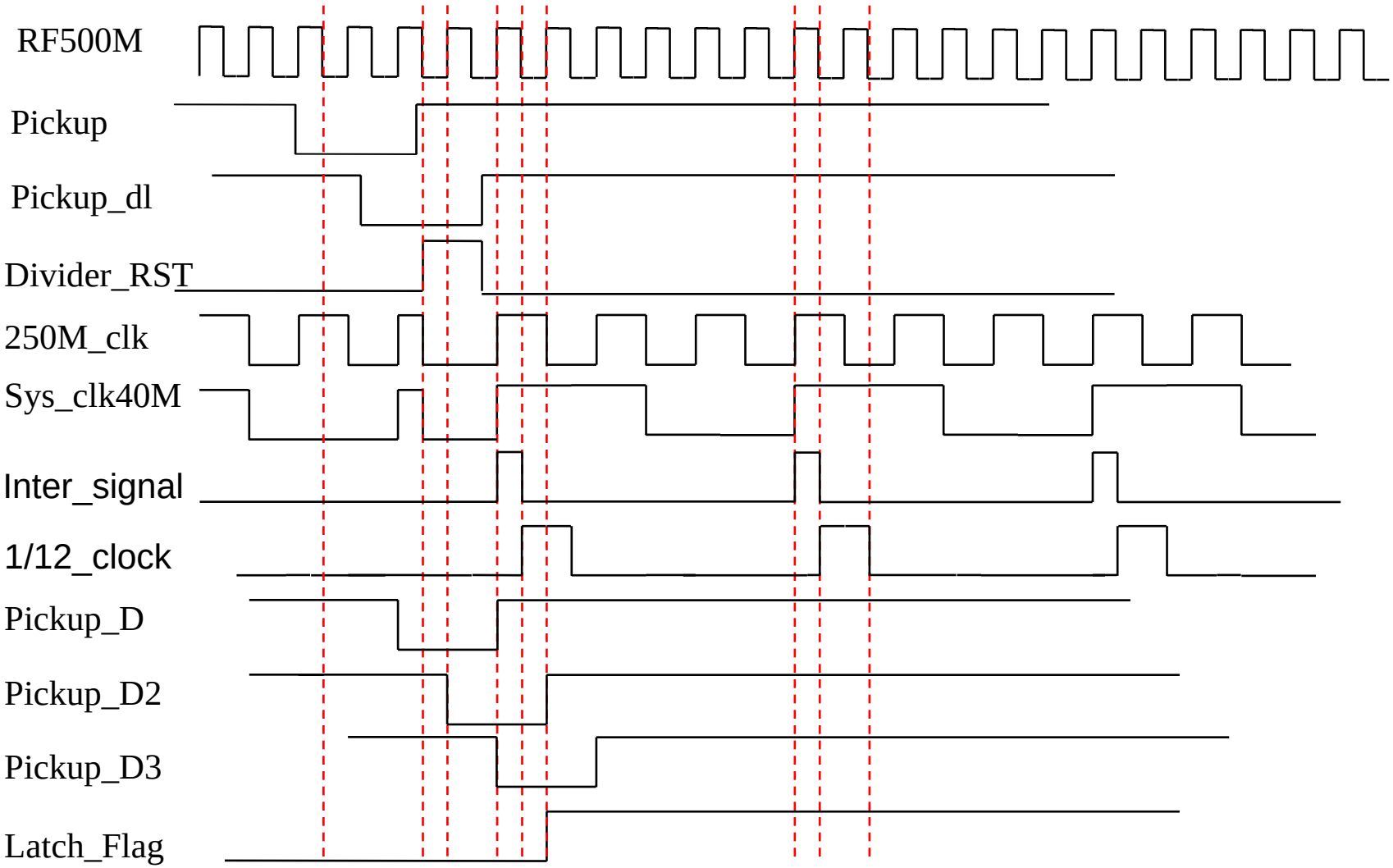
How to Synchronize & Detect It



Schematic of Synchronization Circuit



Ideal Timing Diagram



Performance of ECLinPS Chips

1. MC100EP32 ECL ÷2 divider
   CLK to Q /Q 350~450ps Reset to Q 400~480ps T_{RR} 175ps

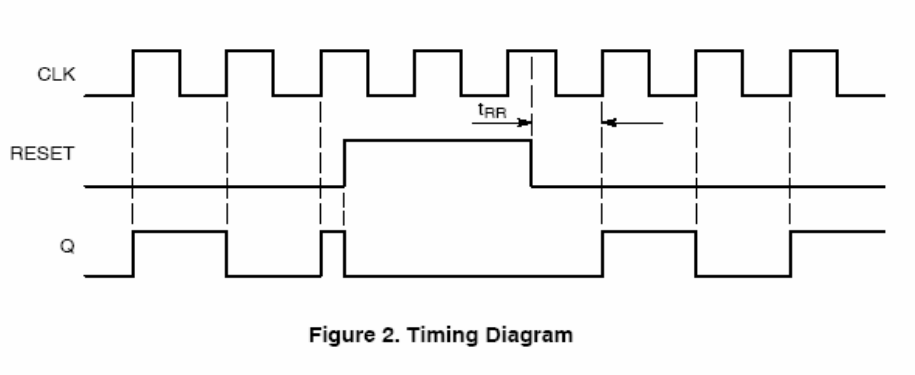
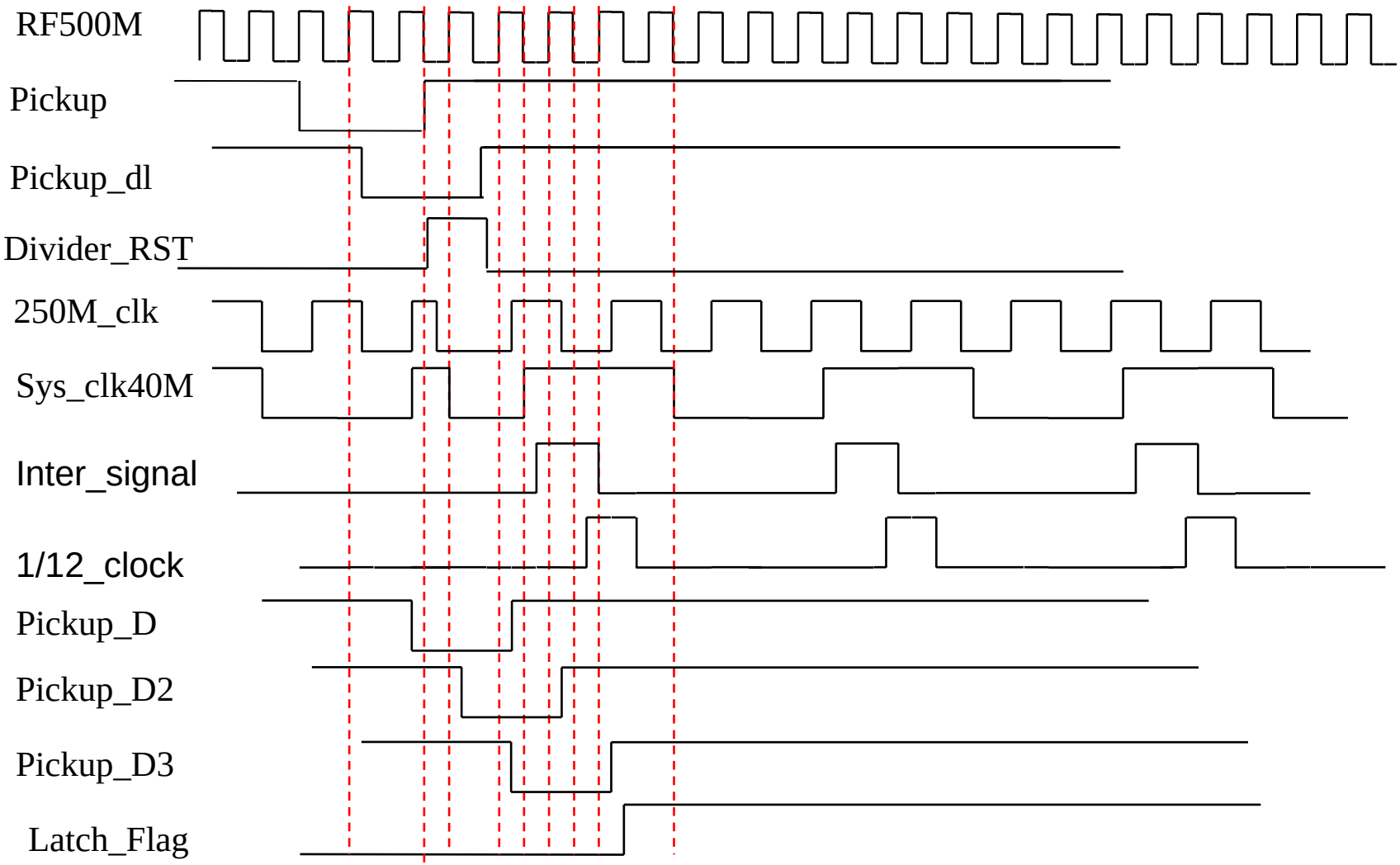


Figure 2. Timing Diagram

2. MC100EP139 ECL ÷2/4, ÷4/5/6 clock generation chip
   CLK to Q /Q 600~900ps Reset to Q 700~1000ps T_{RR} 100~200ps
   t_{Set} /EN->/CLK 120~200ps t_{Hold} /CLK->/EN 50~100ps
3. MC100EP29 dual Differential clock and data Flip-Flop with set and reset
   CLK to Q /Q 420~500ps t_{Set} /t_{Hold} 20~100ps
4. MC100EP131 Quad D Flip-Flop With Set, Reset, and Differential Clock
   C_{0-3} 380~580ps; C_C 400~600ps; R_{0-3} 380~580ps; Set 380~580ps;
   t_{Set}/t_{Hold} 120~80ps

Timing Diagram With Chip's Delay

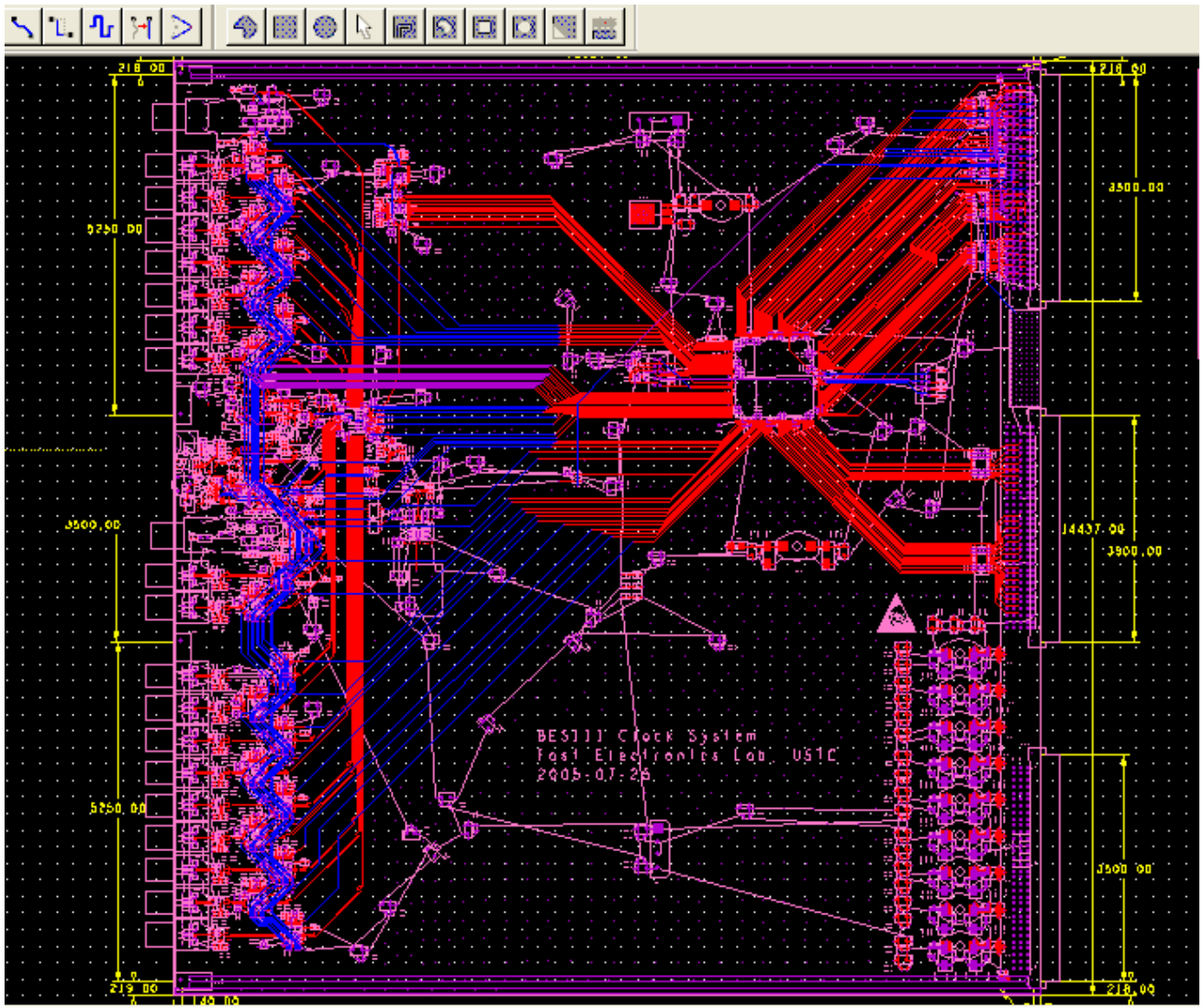


Keystones about the design

1. Time margin
   At least 500ps due to ECLinPS devices
   T_{wire}=2ns-500ps-$Jitter_{pickup}$
   if $Skew_{pickup}$ >500ps, then T_{wire}<1ns !!!

2. PCB layout
   wire delay
   signal integrity

PCB Layout of Clock Generator Module



drawn 4.00, 4.00 apart for enhanced viewability.

Schedule of this task

Schematic design (completed)

PCB Layout (will be completed before 5.10)

Debugging the modules (before 6.10)

Backup module Fabrication (after 6.10)

Thank you