The status of TOF FEE V3.0

Jhguo

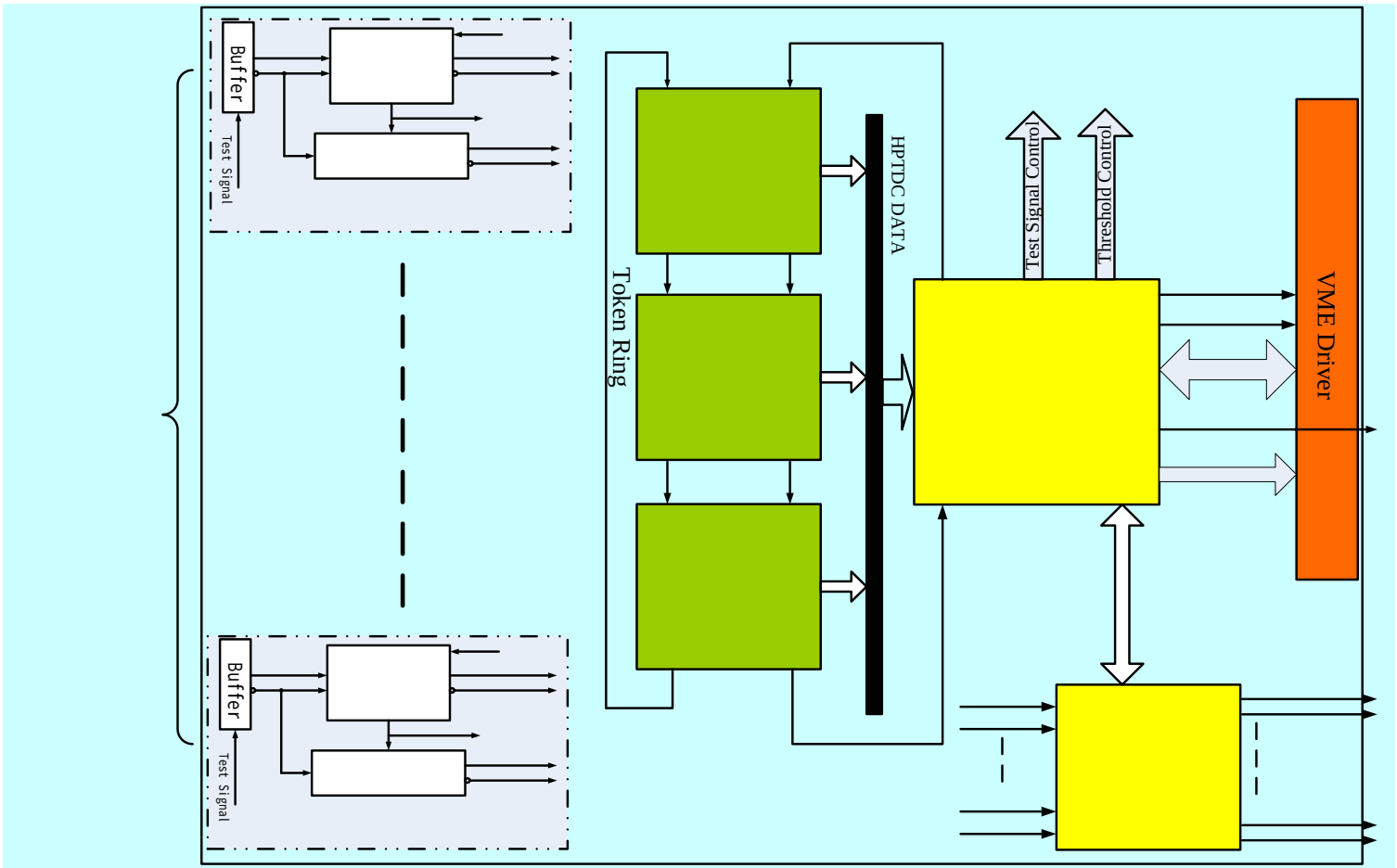
FEL, USTC

2006.4.26

The process of test of FEE V3.0

- 2006.3.21 PCB design finished
- 2006.4.6 begin to solder the chips
- 2006.4.20 begin to test the system

Function diagram of FEE V3.0



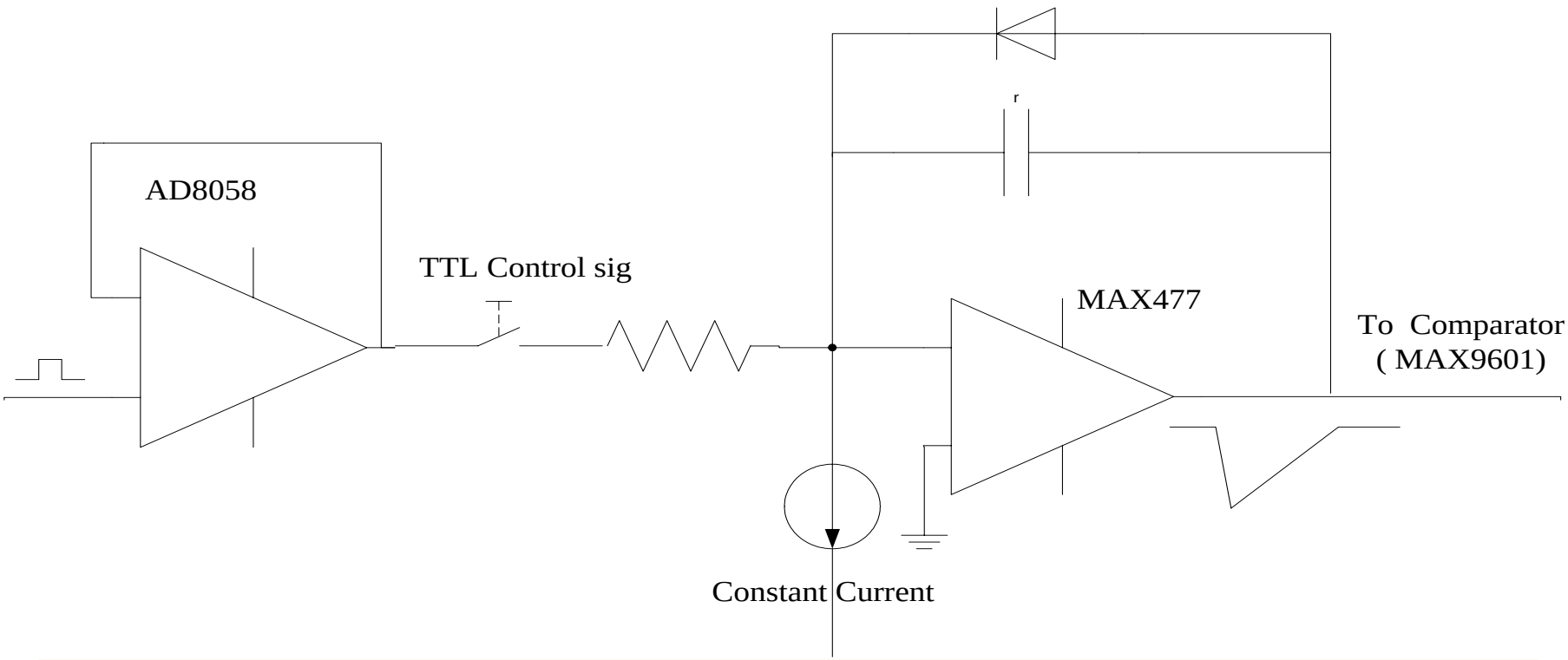

FEE 3.0
FEL.USTC

The improvement of FEE in V3.0

1. use Q-T instead of V-T
2. More Fifo to buffer the event data
   4K WORD deep compared to 2K in V2.0
3. More methods are exploited to mitigate EMI
4. Less power

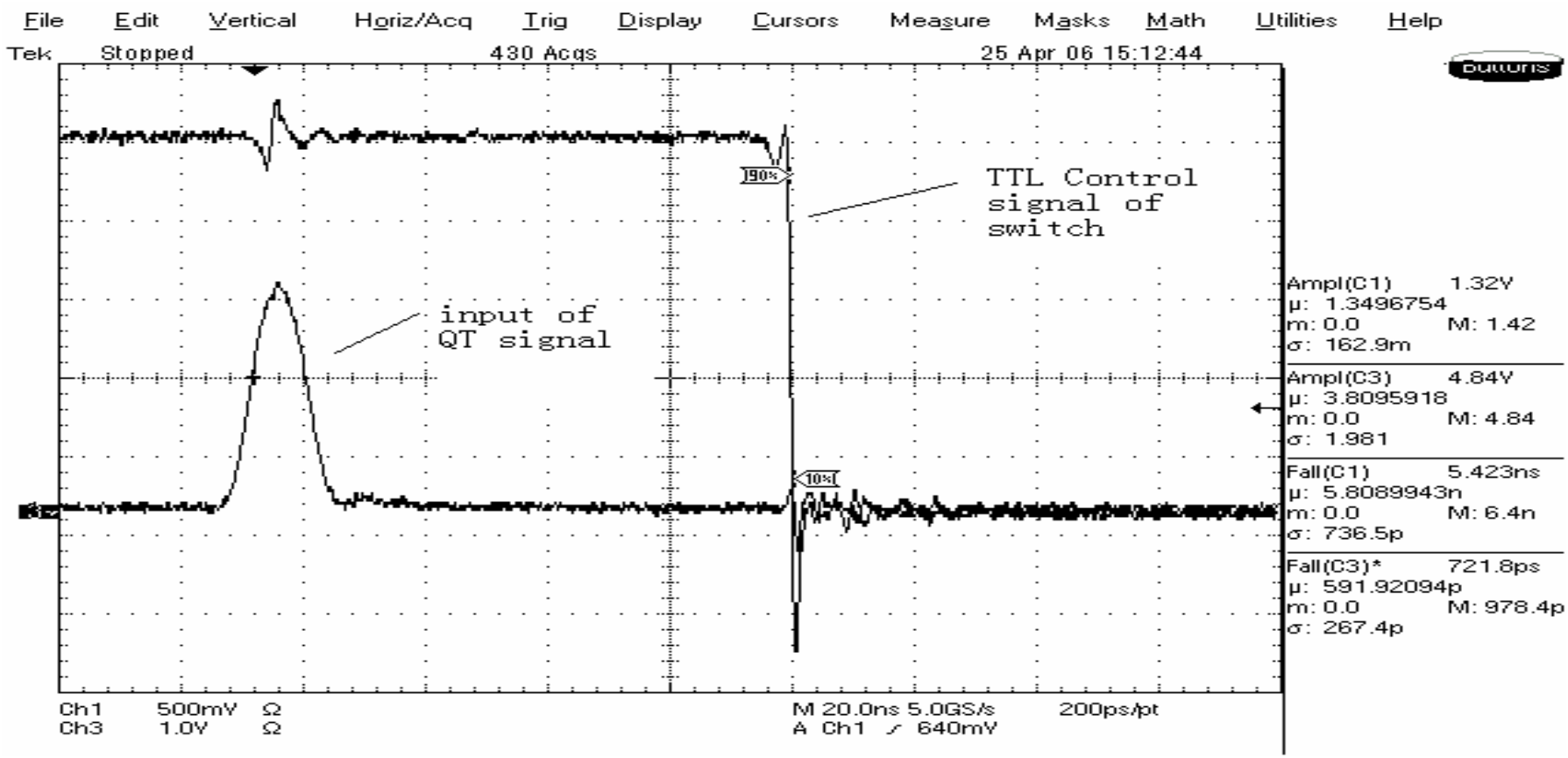
Q-T Circuit of FEE V3.0 (1)

- The capacitance is charged by input pulse and discharged by constant current source.



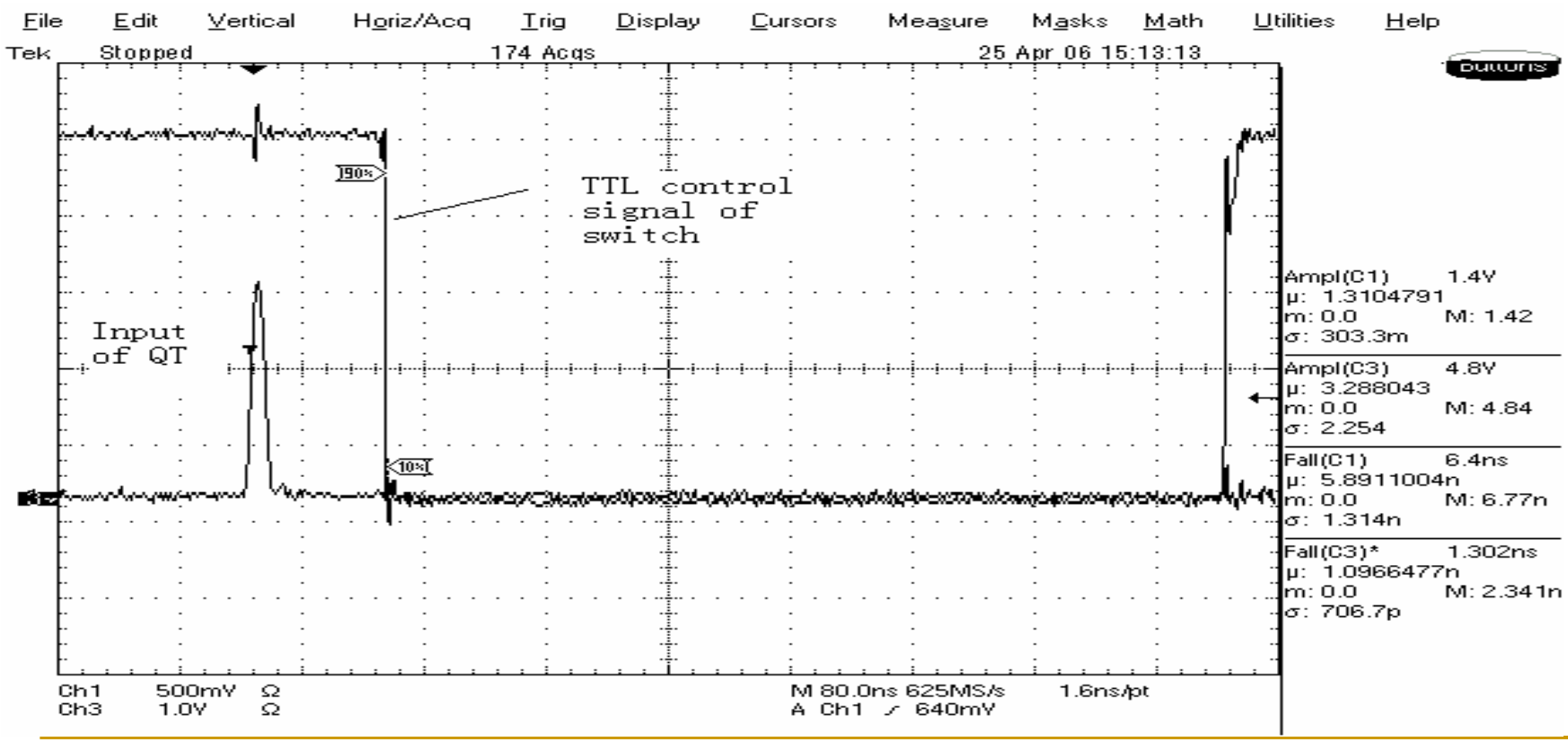
Q-T Circuit of FEE V3.0 (2)

- Timing diagram



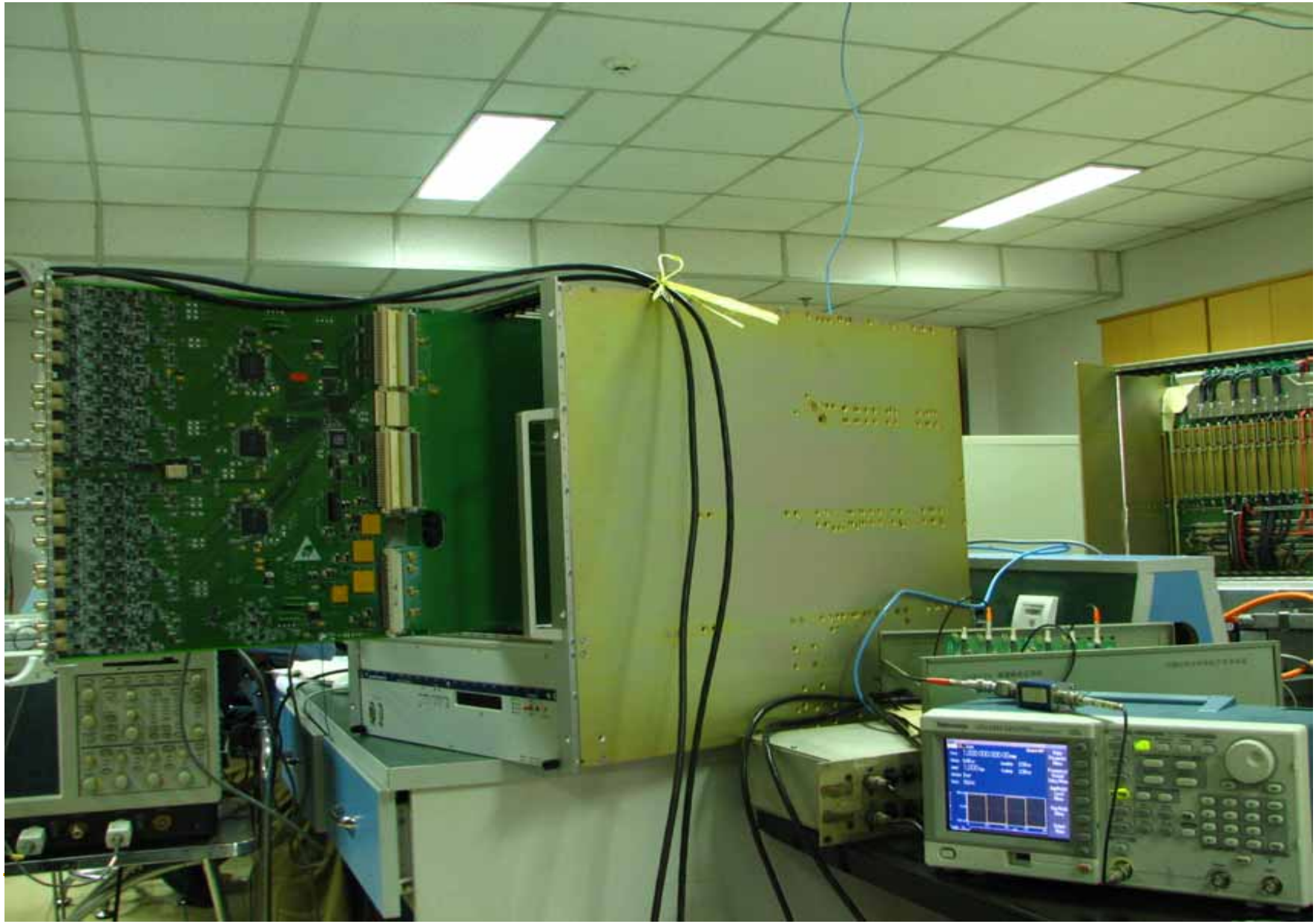
Q-T Circuit of FEE V3.0 (2)

- Timing diagram



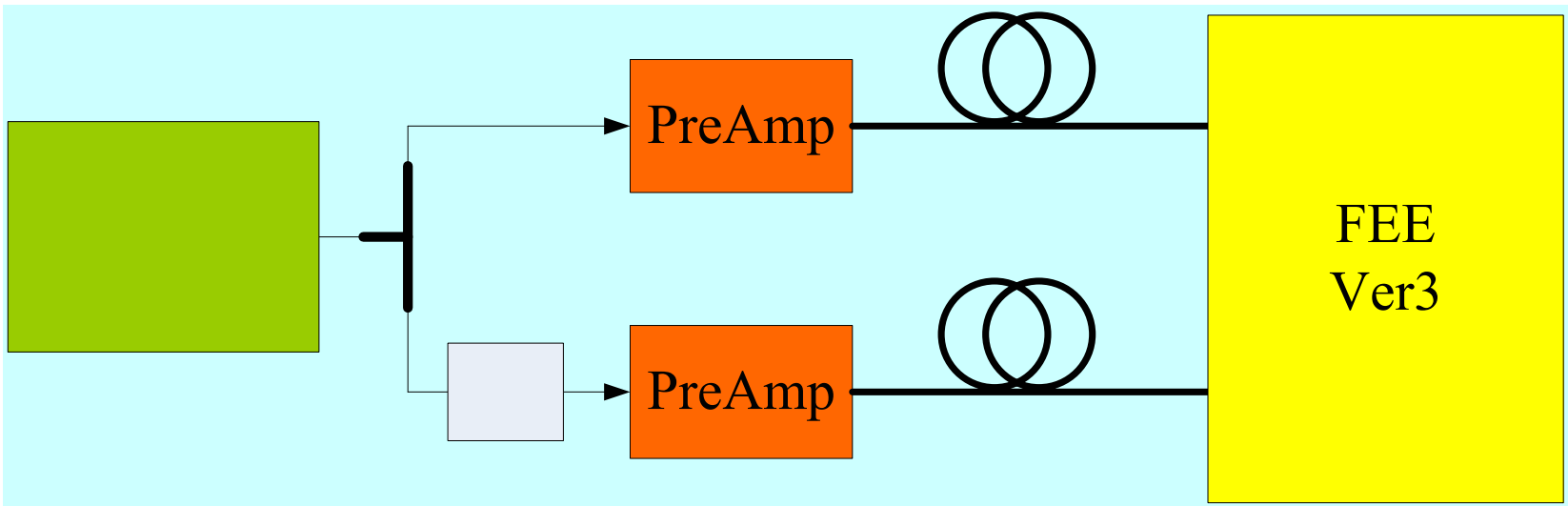
Test of FEEV3.0

- Signal source: AFG3251
  - 14bit resolution
  - 2G/S Arbitrary Waveforms
- oscilloscope
  - TDS7104
- Attenuator:
  - - 12db
- Split:
  - Bandwidth: DC - 2GHz



Test Result(1): time resolution

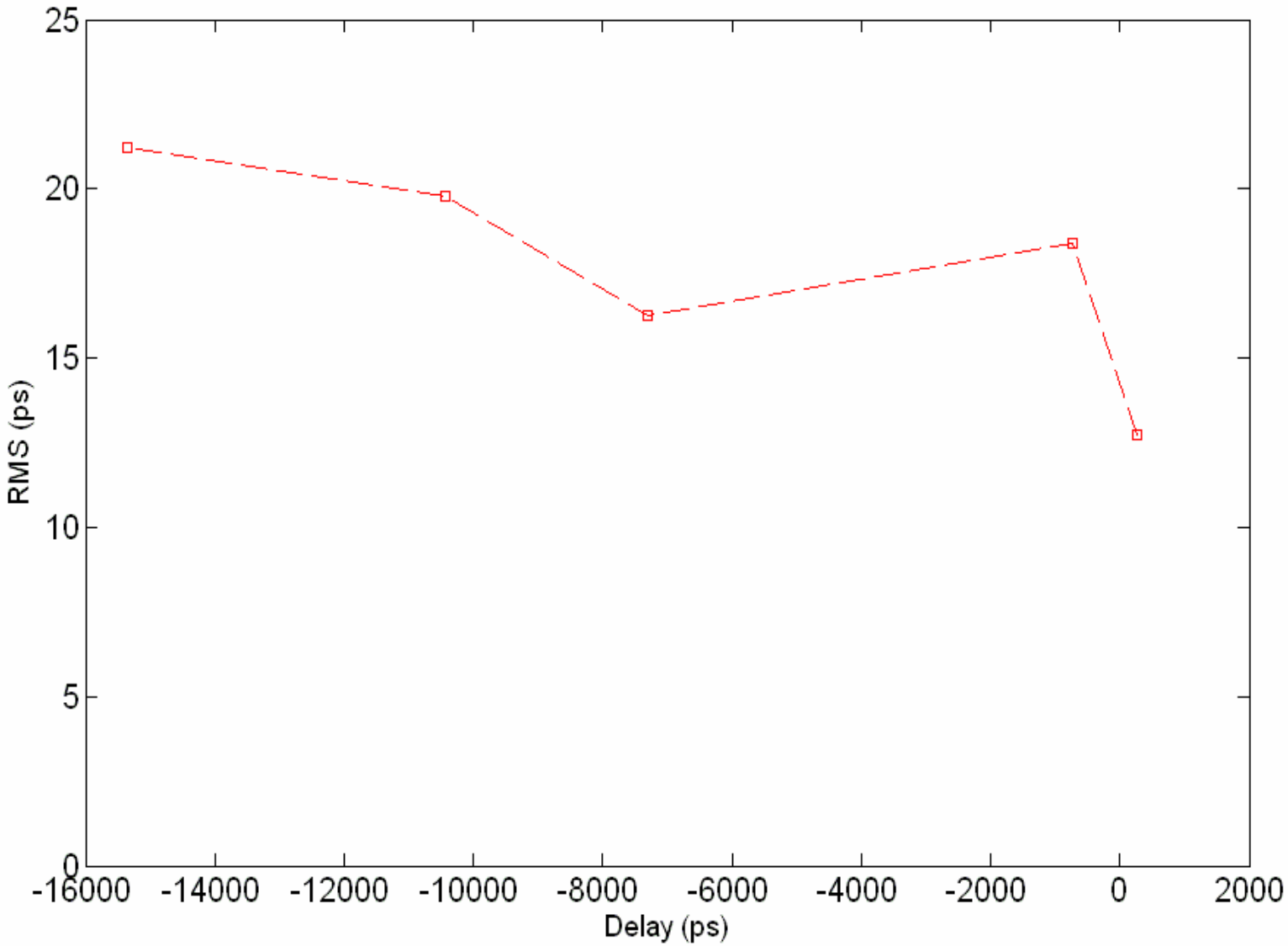
- Test system diagram



Test Result(1): time resolution

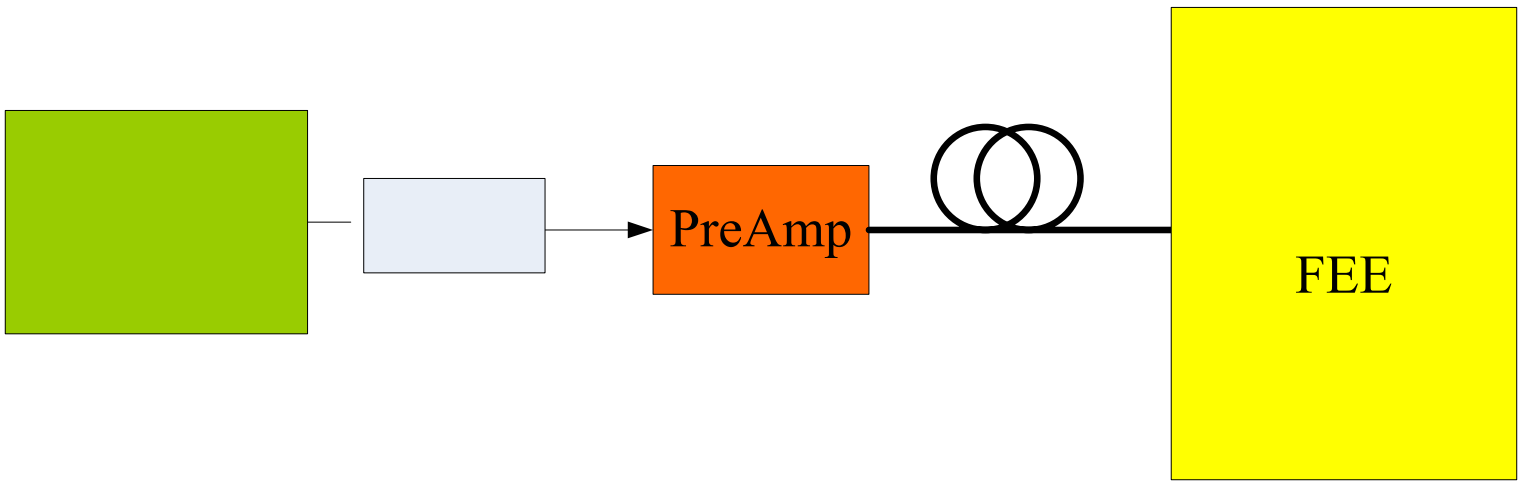
- Condition:
  - LL: 50mv
  - HL:200mv
  - Pulse parameter(AFG3251):
    - Rise time: 5ns
    - Falling time: 5ns
    - Width: 10ns
  - Amplitude: 530mv (single end, at FEE input)

Test Result(1): time resolution



Test Result(2): QT

- Test system diagram



Test Result(2): QT

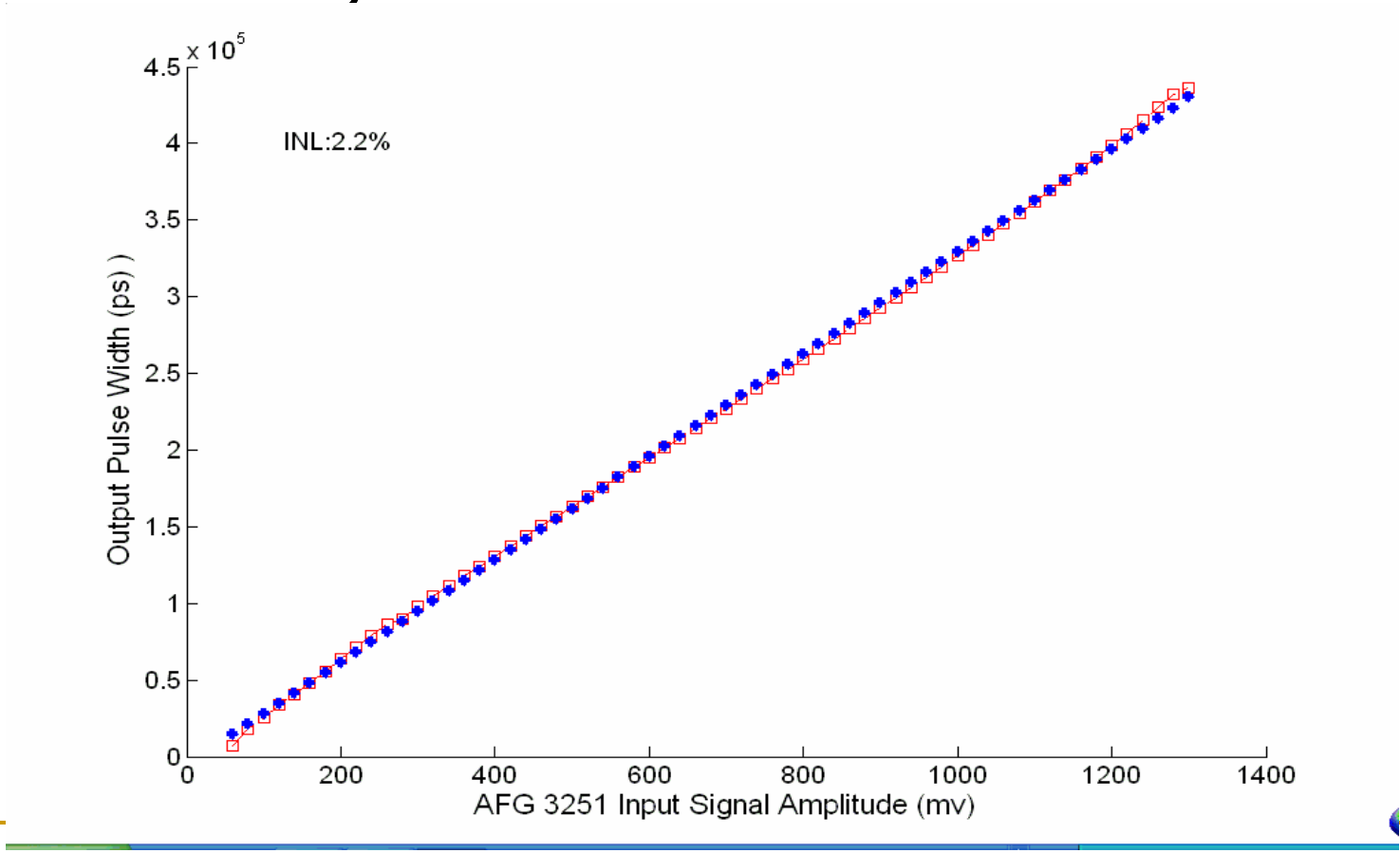
- Condition
  - Pulse parameter(AFG3251):
    - Rise time: 5ns
    - Falling time: 5ns
    - Width: 10ns
    - Amplitude:

      60mv - 1340mv (set of AFG3251)

      62mv - 1.48V (single end, at FEE input)

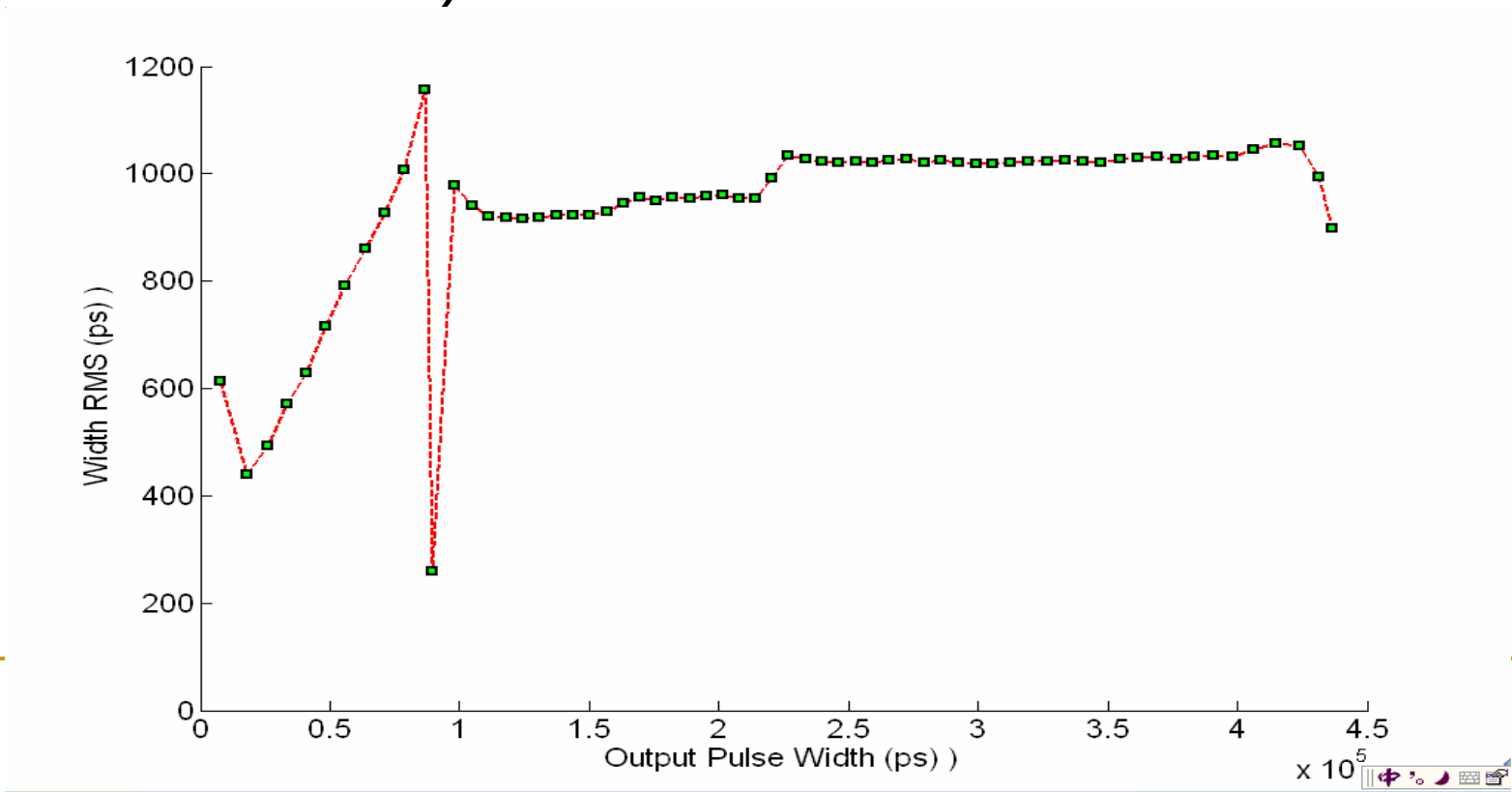
Test Result(2): QT

- Nonlinearity



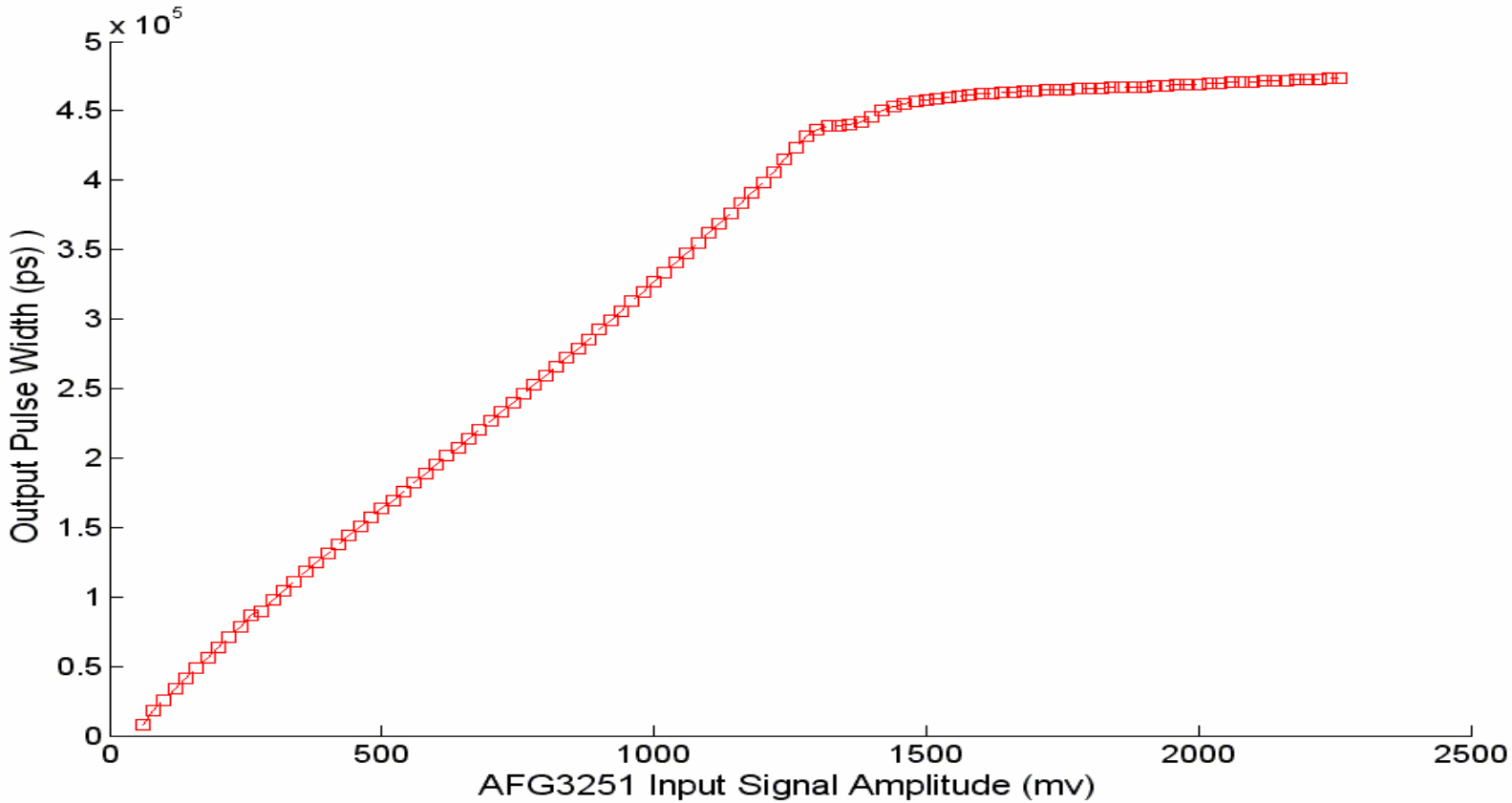
Test Result(2): QT

- RMS
  - Each QT bin is 100ps, 12 bit (dynamic range is about 400ns)



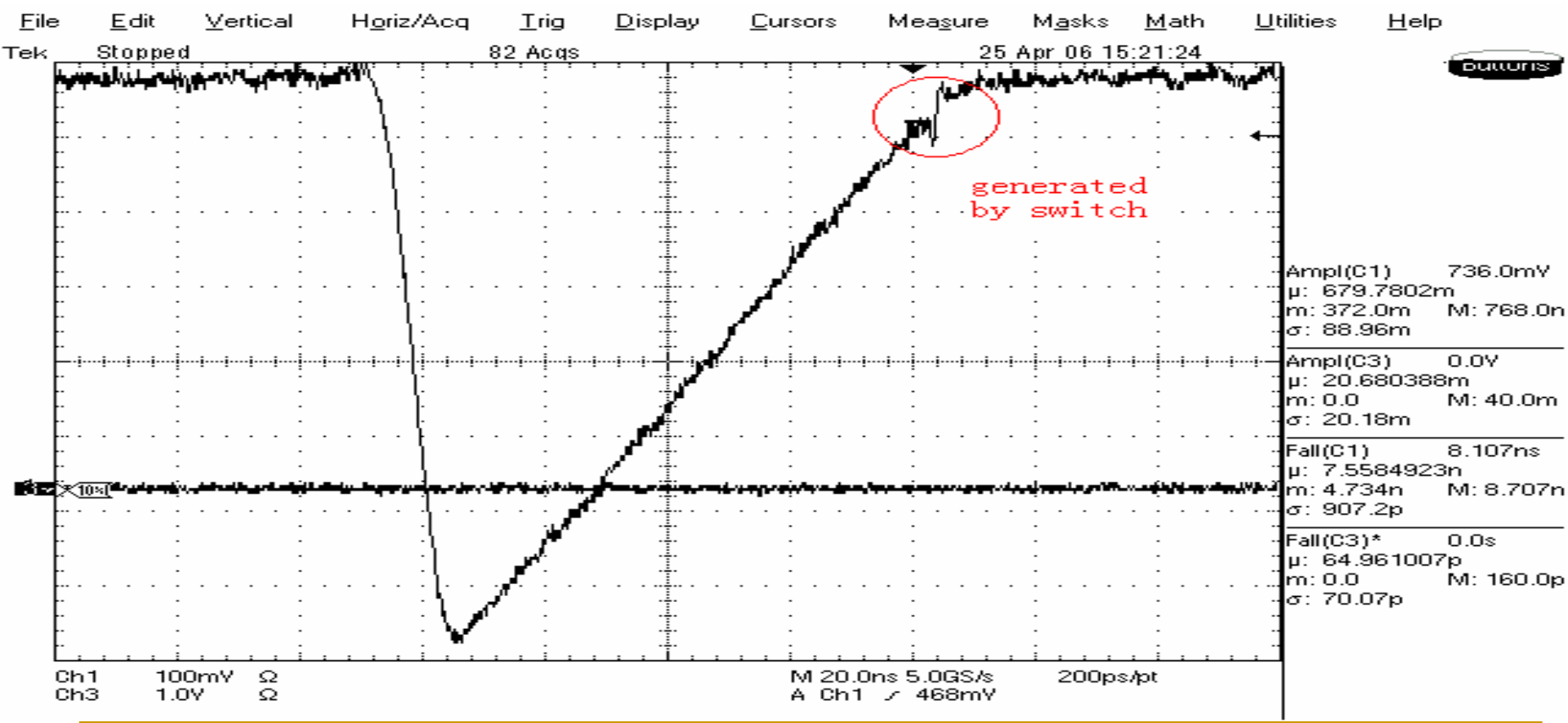
Test Result(2): QT

- Saturation of QT



The problem of QT circuit

- Influence of the switch of QT circuit



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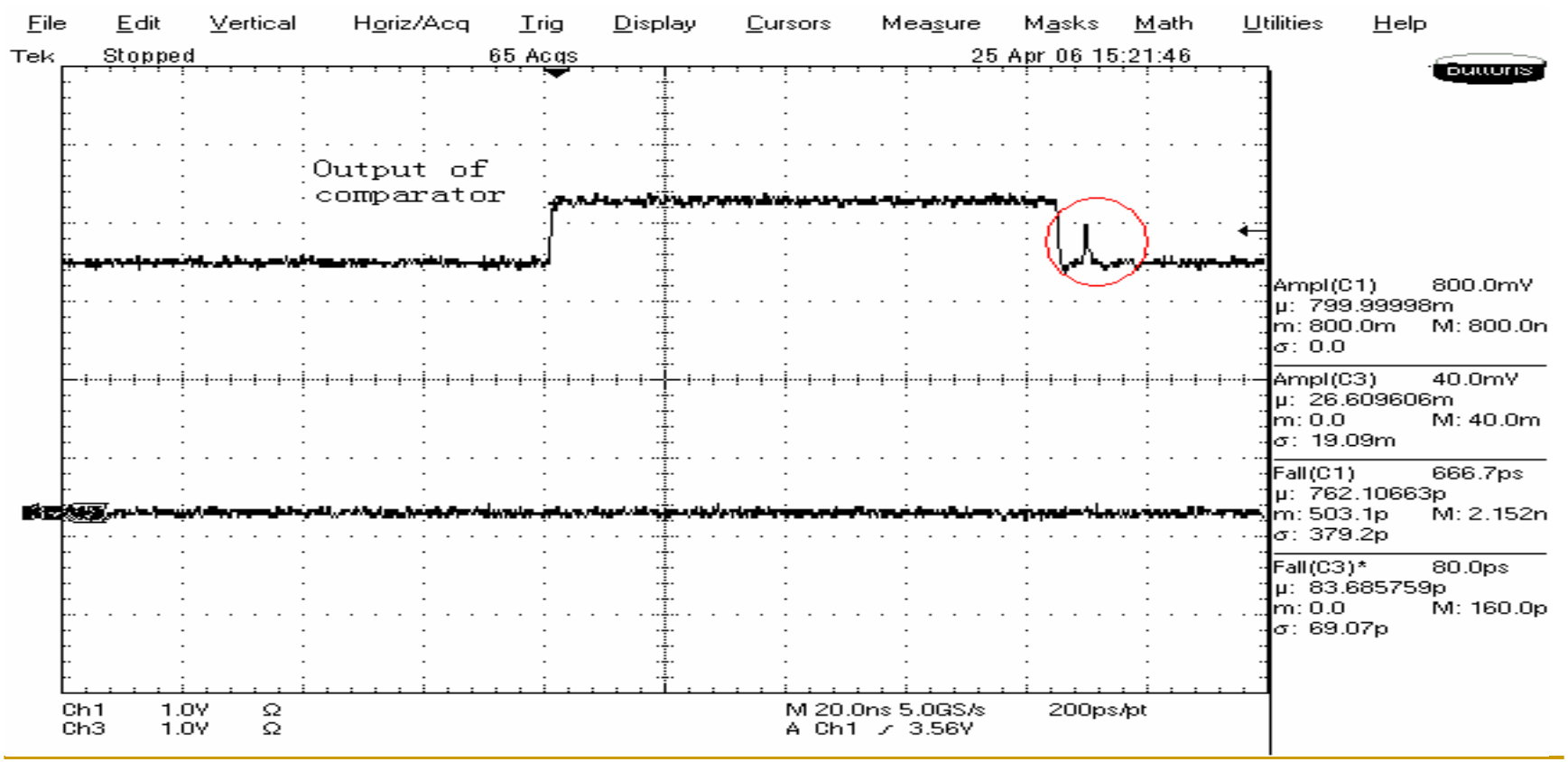

The problem of QT circuit

- The L1 Buffer of HPTDC may be full?
  - The L1Buf of HPTDC is 256 WORDs deep, and it is shared by 8 channel.
  - When the QT result wait for L1 trigger, the L1 Buffer of HPTDC may be full?

The power of FEE V 3.0

- +3.3V: 2A
- +5.0V: 9A

  (about 4.85V at FEE board, because of resistor of fuse)
- -5.2V: 2A
- -12V: 0.2A

More test will be done

- Cross talk test
- Stability test
- More FEEs will be assembled and Cosmos ray test are scheduled

Thank you!