Modification for Fast-Control Module & FEE-Rear Module

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Outline

- Fast-Control Module
  -Basic Functions of Fast-Control Module
  -Former Version
  -Modifications in the new version

- FEE-Rear Module
  -Basic Functions of FEE-Rear Module
  - Former Version
  - Modifications in the new version

Functions of Fast-Control Module

-Receive fast control signals by fiber and fan them to FEE modules in the crate.

-Collect FEE status signals via VME reserved bus and transmit them to Trigger System by fiber.

Old Fast-Control Module

- The number of control signals is 9.
- The number of status signals is 5.
- All these signals in the crate are collected and fanned out via VME reserved bus.

Three Main Modifications

- An external L1 signal is requested
  - LVDS signal from a LEMO connector
  - Used for monitor modes

- The number of control signals is increased to 10
  - A new control signal ,FEE-System-Reset, is appended
  - Net name: FEERST
  - VME MCTL(J1.Z9).

- The number of status signals is increased to 6
  - A new status signal ,FEE-Config-Done, is appended
  - an OD signal from FEE boards
  - Net name: FEECongfigOK
  - VME MMD(J1.Z7)

		Net Name	VME Pin	FPGA Pin	Function Description
10 CONTROL SIGNALS	D0	L1	J1.Z23	Pin101	Trigger signal
	D1	CHK	J1.Z21	Pin104	Check
	D2	RST	J1.D21	Pin103	Reset
	D3	RLOAD	J1.Z19	Pin106	FPGA Config Rload
	D4	FRST	J1.Z17	Pin107	Fiber Reset
	D5	TSYNC	J1.D19	Pin105	Trigger synchronization
	D6	TPD0	J1.Z13	Pin114	Reserved
	D7	TPD1	J1.Z15	Pin113	Reserved
	D8	CRSV	J1.D23	Pin100	Reserved
	D9	FEERST	J1.Z9	Pin115	FEE Reset From DAQ

		Net name	VME Pin	FPGA Pin	Function Description
6 Status signals	D0	FULL	J1.Z25	Pin74	FEE Buffer Full
	D1	SRSV	J1.Z27	Pin65	Reserved
	D2	FUERR	J1.Z29	Pin56	Reserved
	D3	FDERR	J1.Z31	Pin55	Reserved
	D4	TDC_OVERFLOW	J1.D25	Pin78	TDC Overflow
	D5	FEE_ConfigDone	J1.Z7	Pin132	FEE Config Done

Other Modifications

- 1)Use FPGA EP1C6Q240C8 to replace EPF10K30A.
- 2) VME Interrupts is applied for future extension.
- 3)D16-D31 of VME Data Bus is also applied for future extension.

Other Modifications (cont.)

- 4)Use a Multiplexer-Driver to replace the clock jumper.

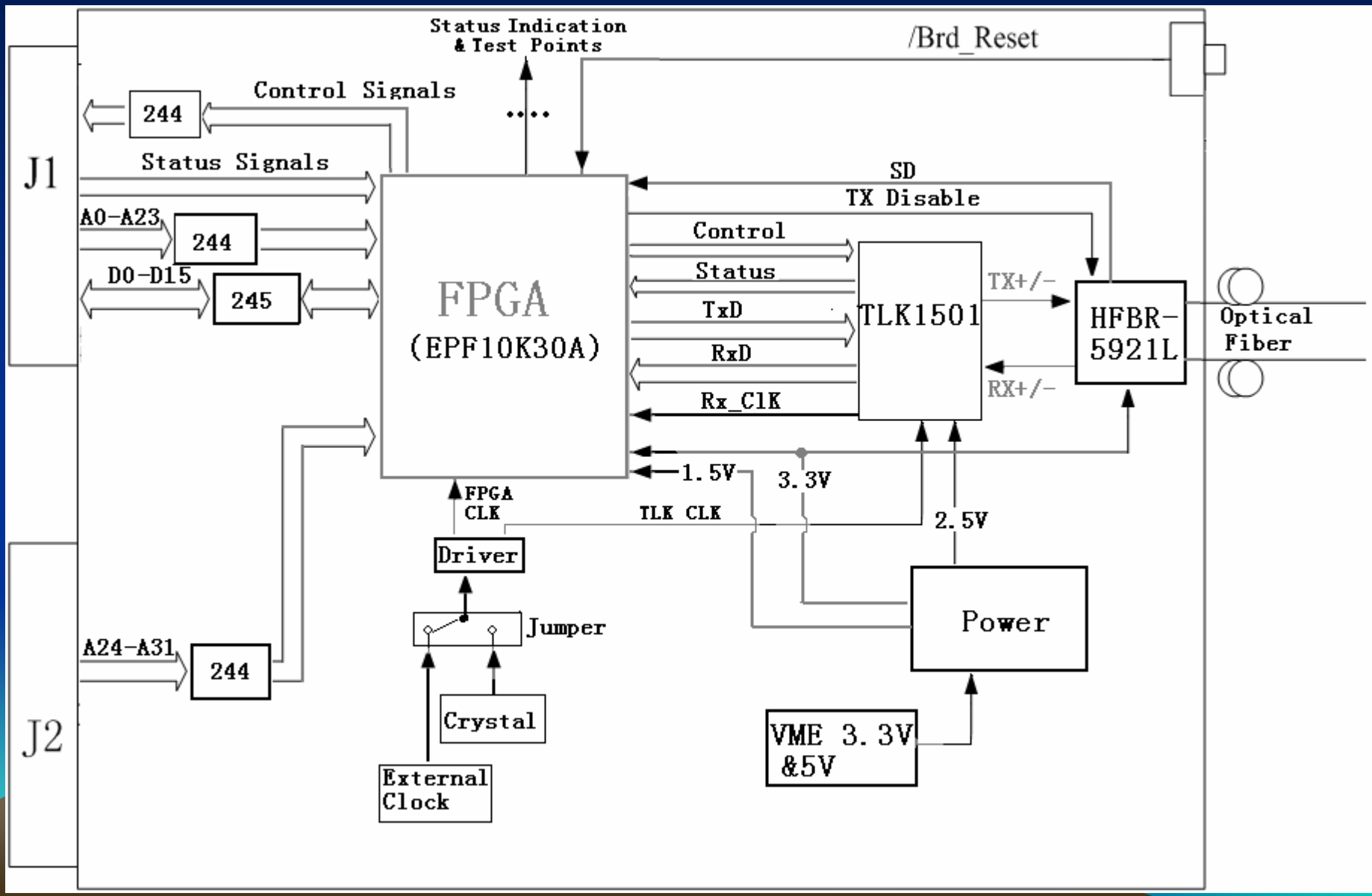
  -This makes the module more flexible.

- 5)Power-supply part is also reconsidered.

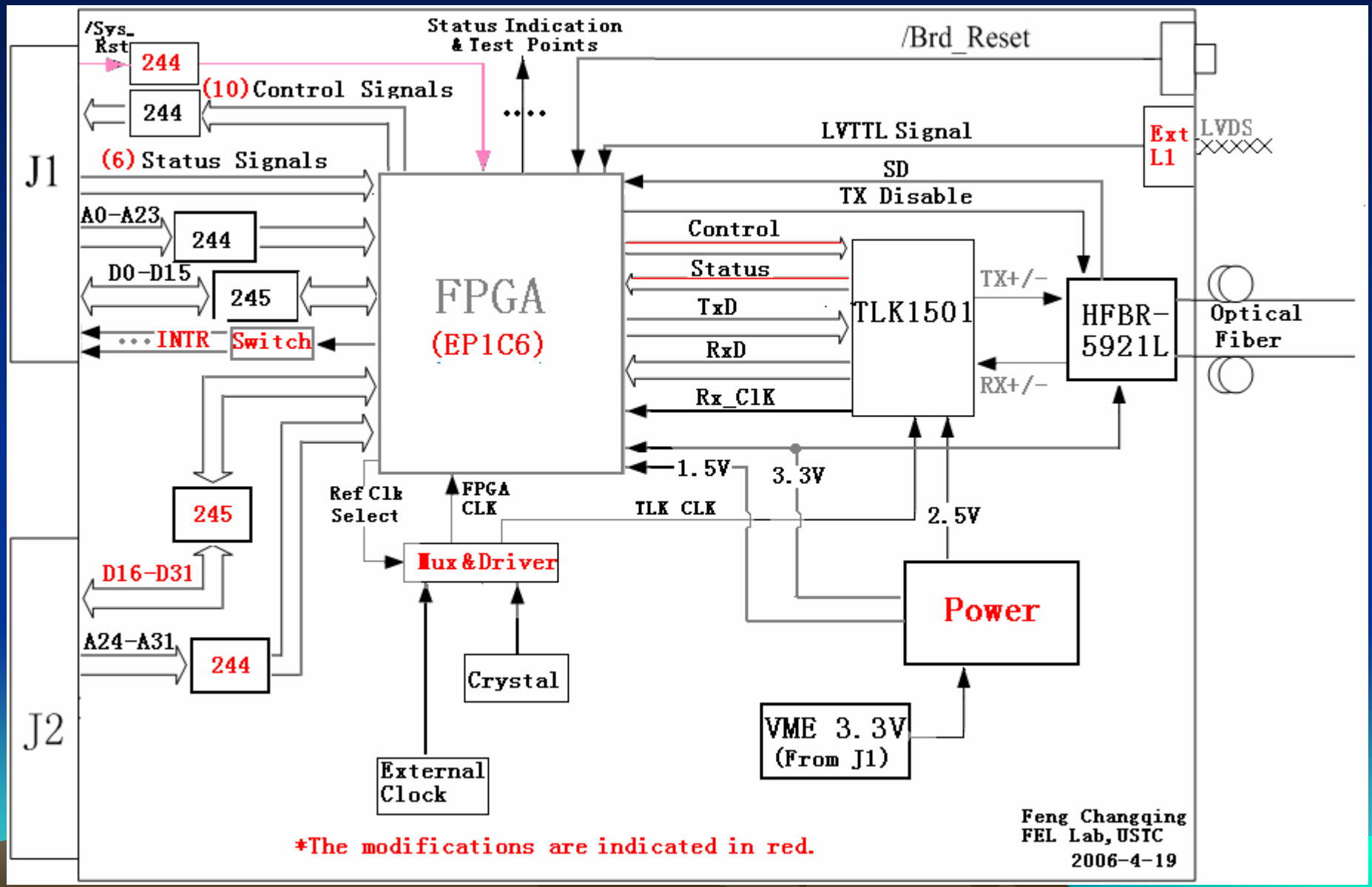
- 6) Some pins of TLK1501 is connected to FPGA directly

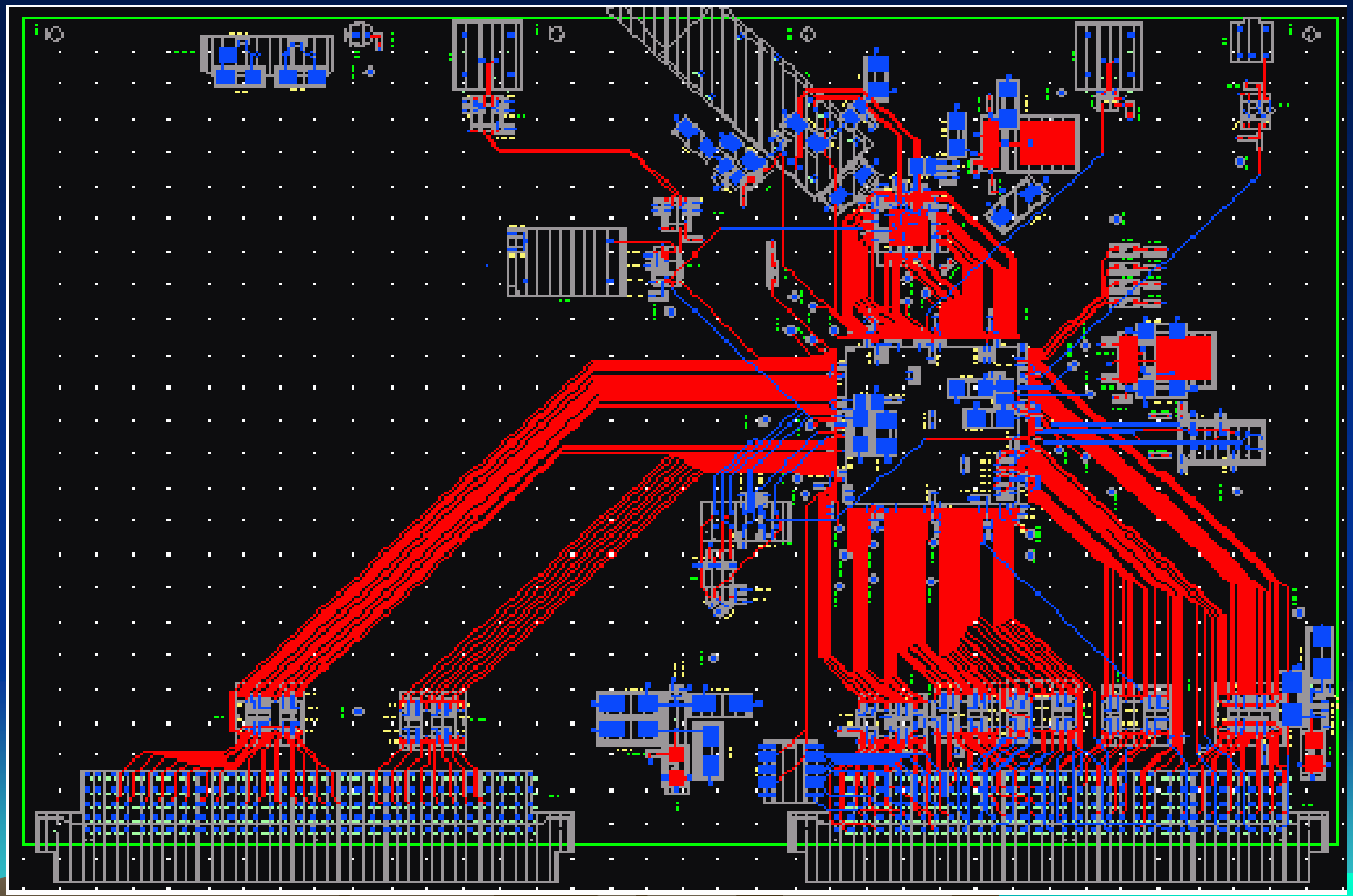
  (LOOPEN,ENABLE,LCKREFN,PRBSEN)

Diagram of Former Fast-Control Module



Schematic Diagram of new version





Functions of FEE-Rear Module

- Receive Mean Timer Signals from TOF-FEE Module.
- Send Mean Timer Signals to TOF Trigger System.

Main Modifications

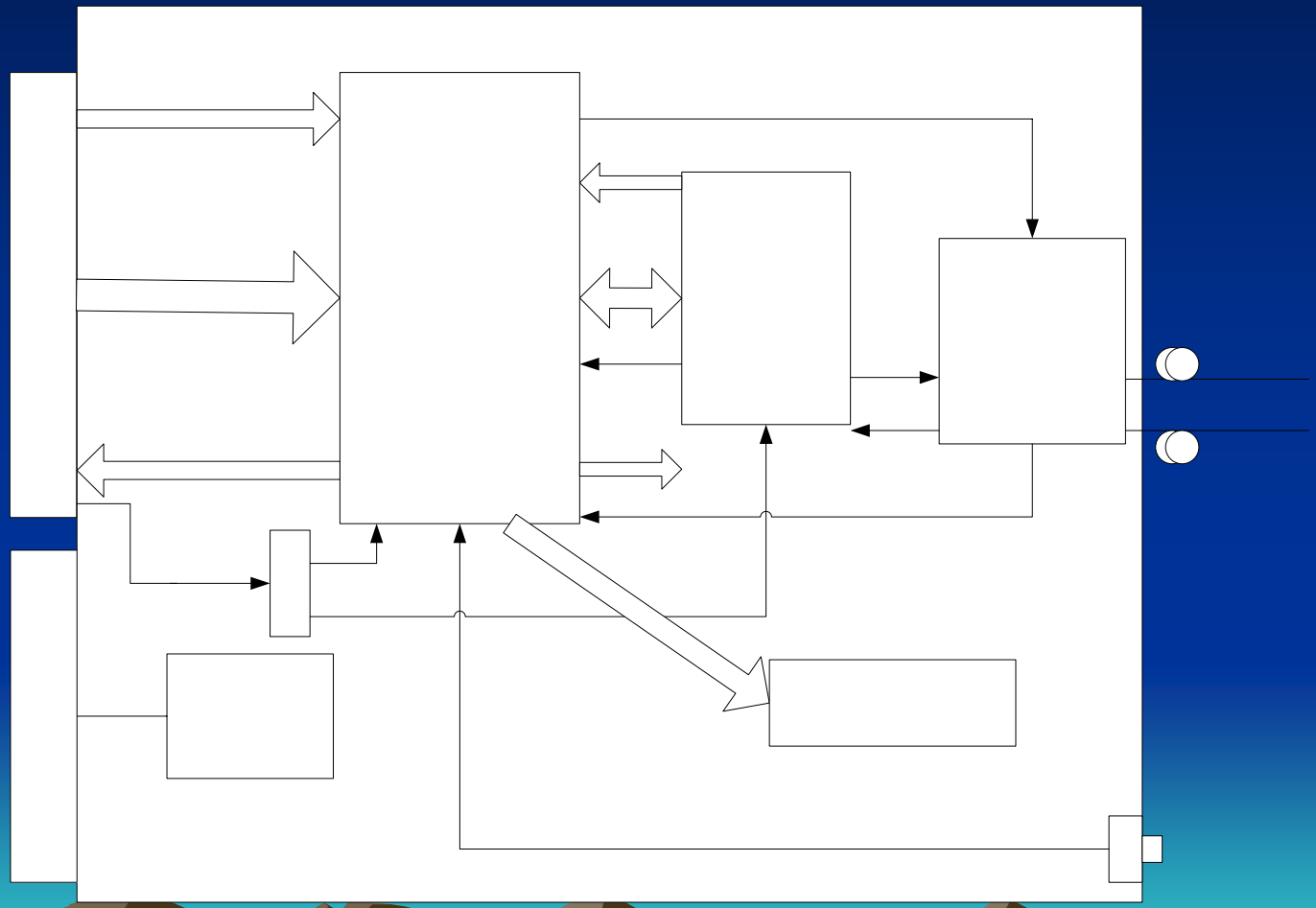
- Old FEE-Rear module only send mean timer signals by fiber.
- LVDS transfer of mean timer signals is requested in new module

  -by twisted cables

Other Modifications

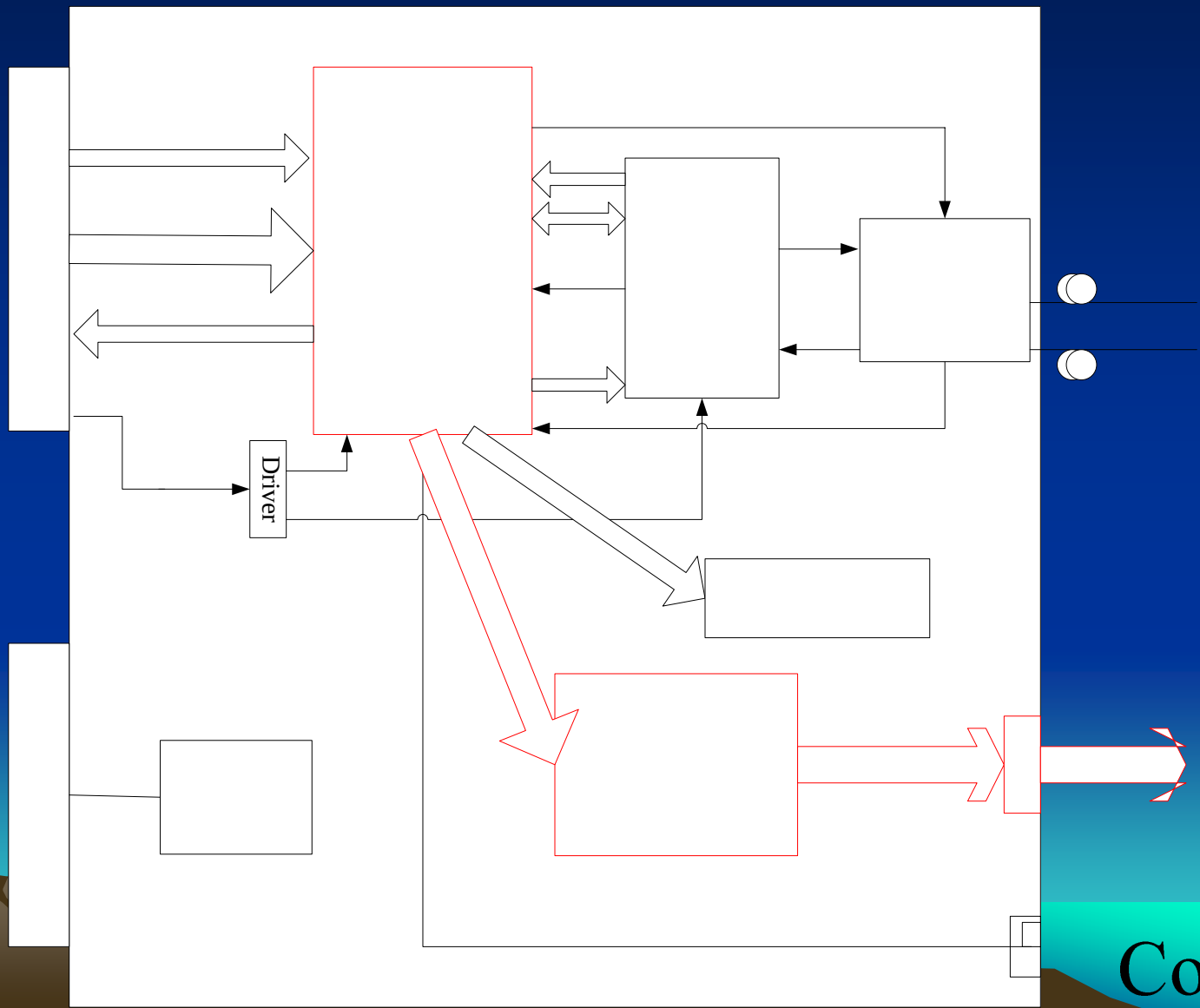
- 1)Apply Altera FPGA EP1C6Q240C8 to replace EP1C3T144C8 .
- 2)Apply TI SN65LVDS387 as LVDS transmitter
- 3)Apply Box Header With Ejectors 2.54mm as the connecter.
- 4)Apply Twist “n” Flat Speed bloc® IDC Ribbon Cable as the cable.

Former FEE-rear-Board Diagram

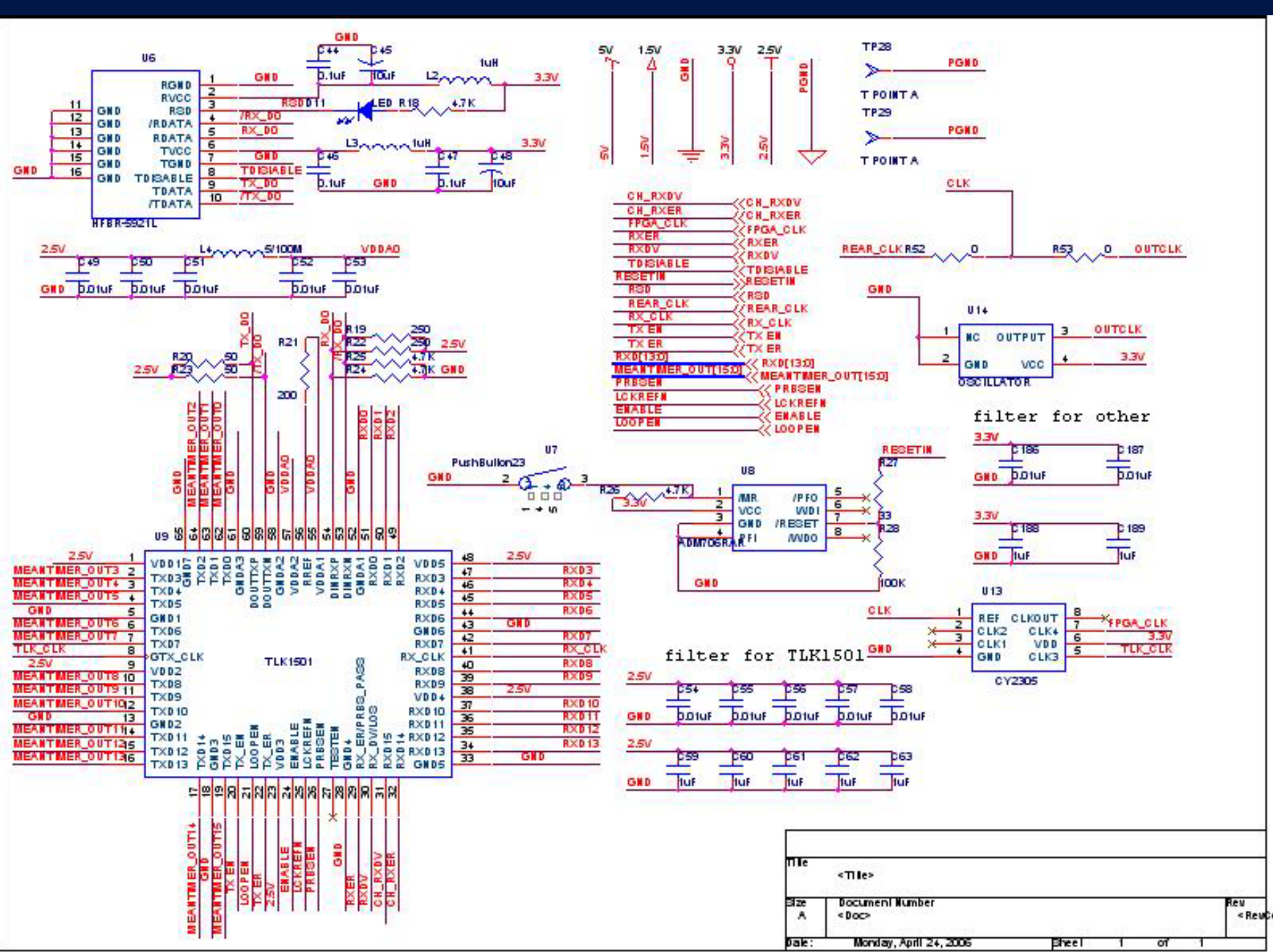


Control Res

New Vision



Control,



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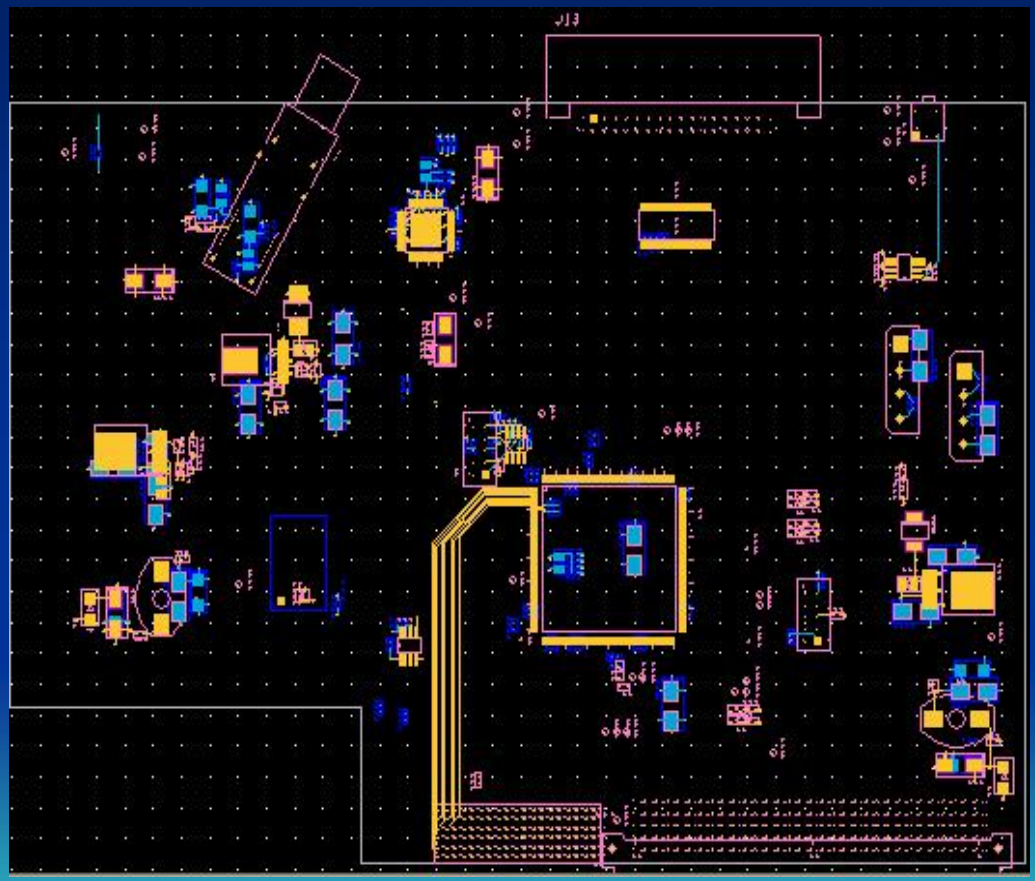
Date: Monday, April 24, 2006	Sheet 1 of 1	

Thanks !

PCB Layout of FEE_Rear 3.0



Schedule

- Fast-Control

  -PCB layout: is completed now

  -PCB manufacture: early May

  -Test: Before early July

- FEE-Rear

  -PCB layout: is to be finished before the middle of May